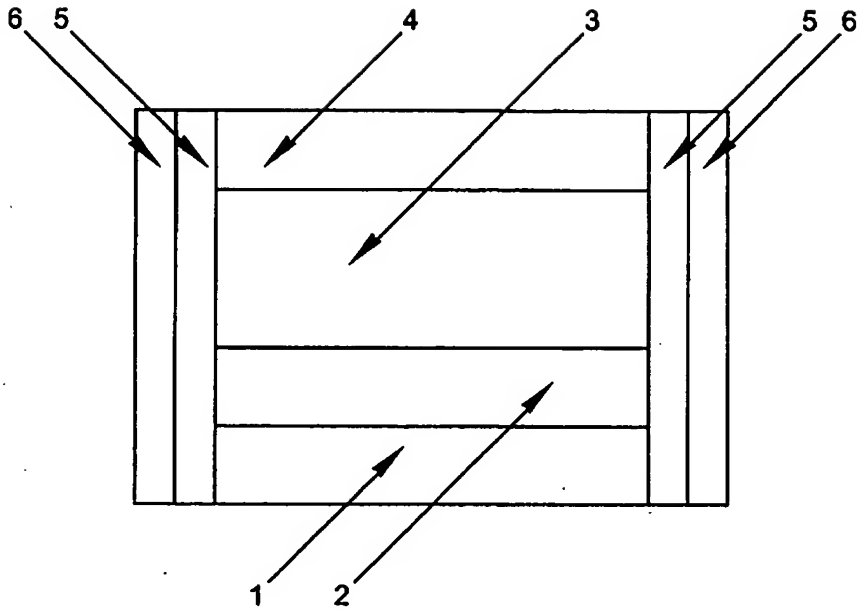


Figure 1

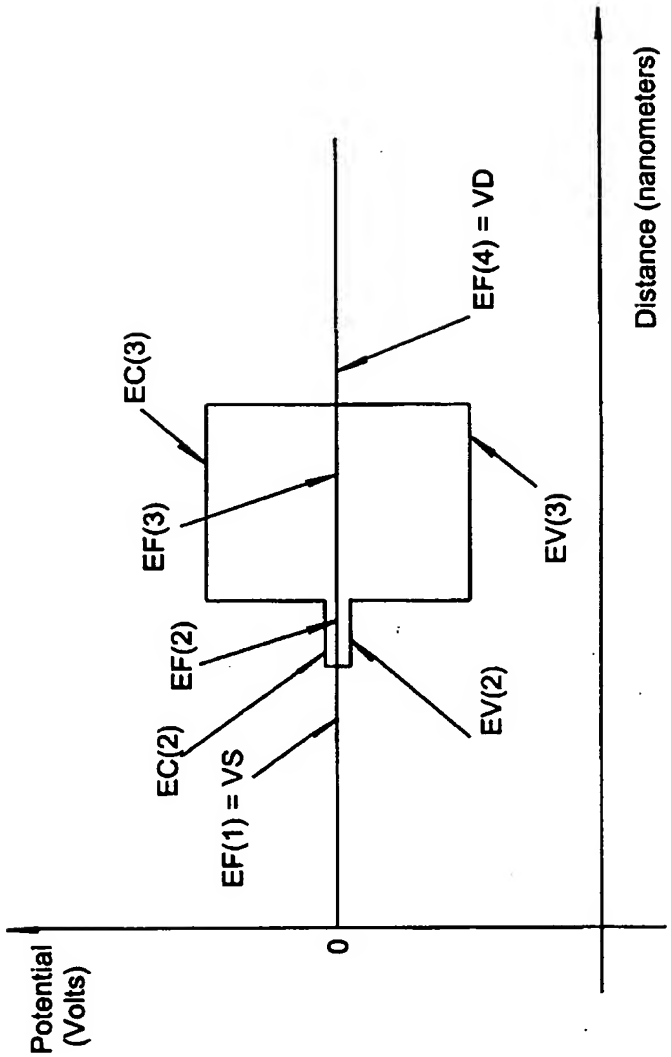

Potential (Volts)
0
Distance (nanometers)
EC(3)
EF(3)
EF(2)
EC(2)
EF(1) = VS
EF(4) = VD
EV(3)
EV(2)

Figure 2a

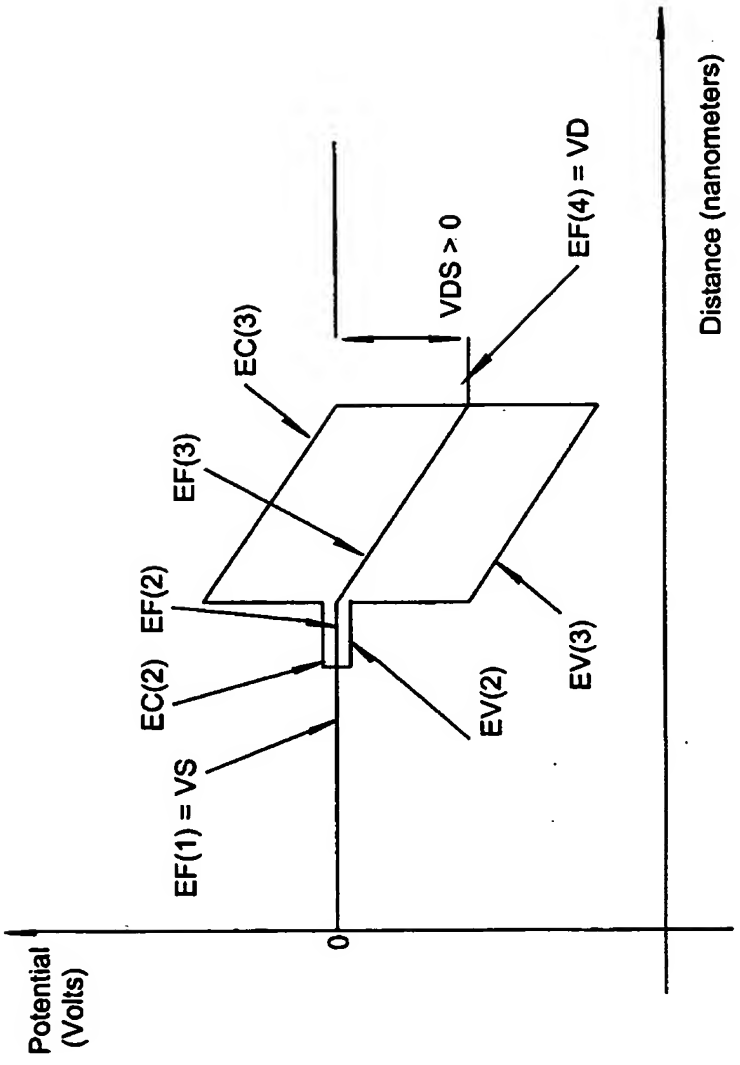

Potential (Volts)
Distance (nanometers)
0
EF(1) = VS
EC(2)
EF(2)
EF(3)
EC(3)
VDS > 0
EF(4) = VD
EV(2)
EV(3)

Figure 2b

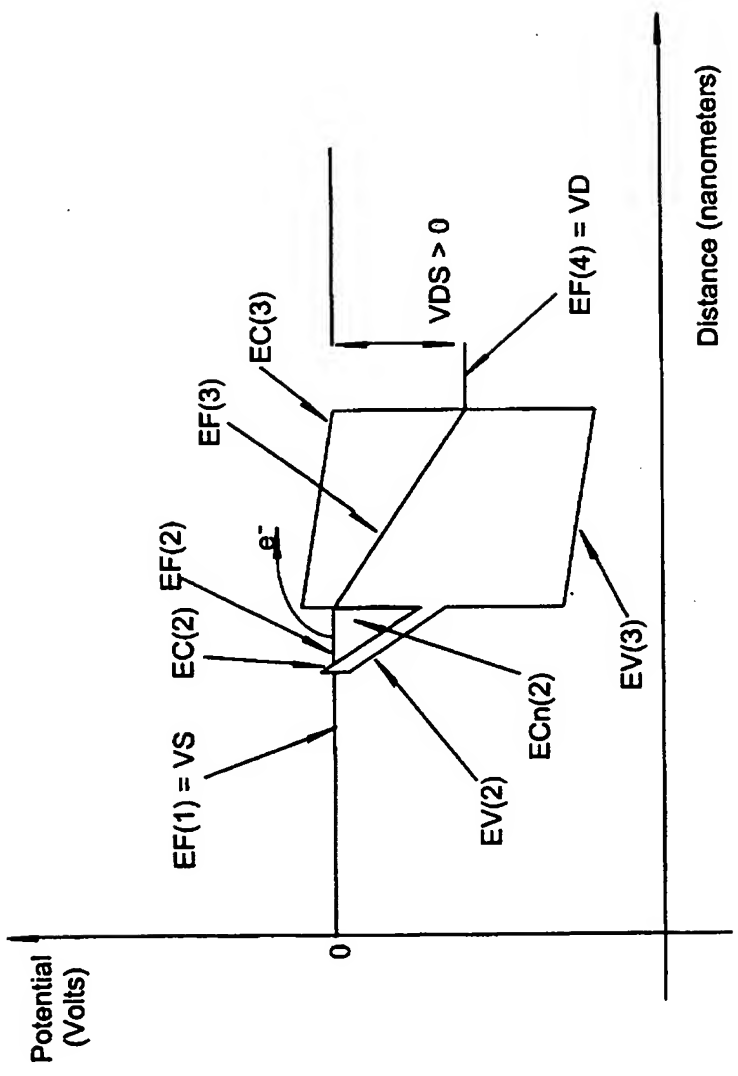

Potential (Volts)
0
Distance (nanometers)
EF(1) = VS
EC(2)
EF(2)
e-
EF(3)
EC(3)
VDS > 0
EF(4) = VD
EV(2)
ECn(2)
EV(3)

Figure 2c

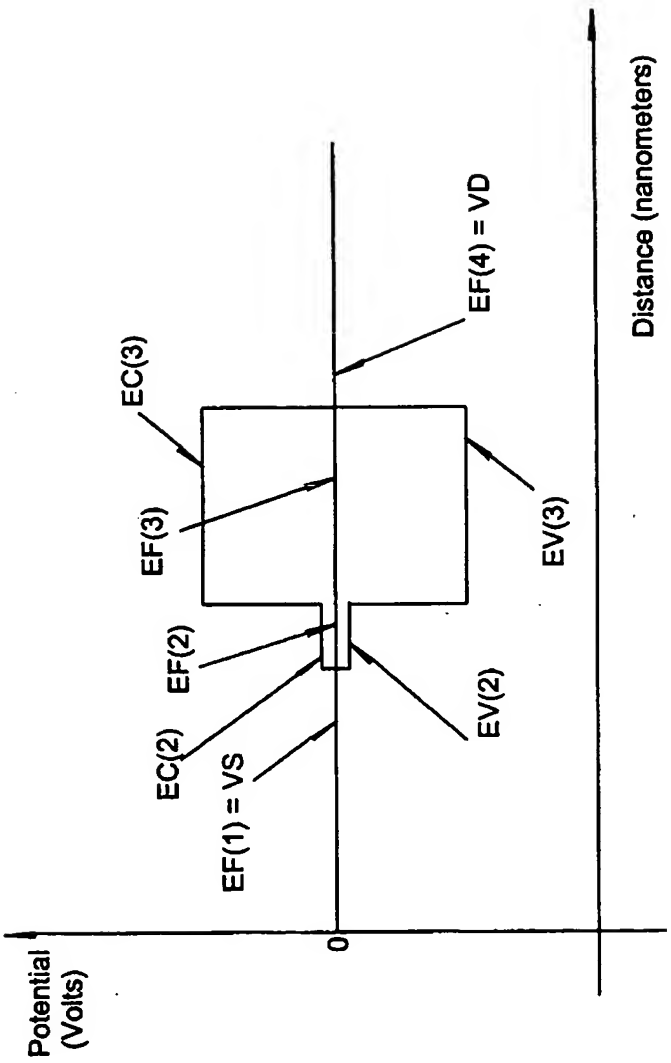

Potential (Volts)
Distance (nanometers)
0
EC(3)
EF(3)
EF(2)
EC(2)
EF(1) = VS
EF(4) = VD
EV(3)
EV(2)

Figure 3a

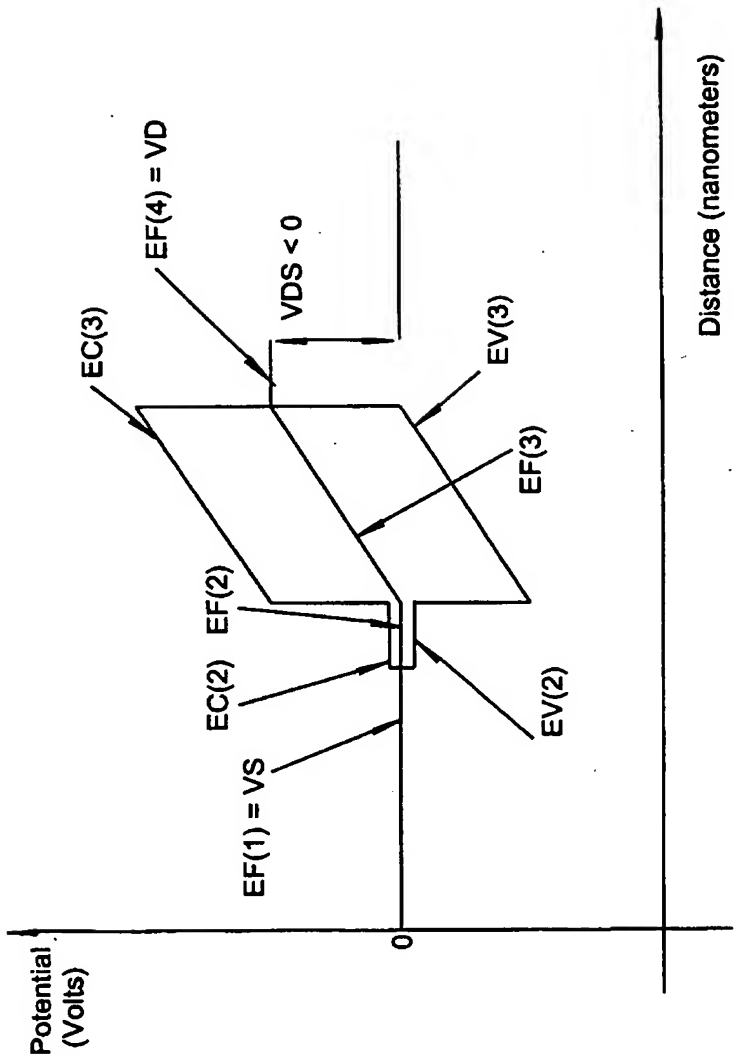

Potential (Volts)
0
EF(1) = VS
EC(2)
EF(2)
EC(3)
EF(4) = VD
VDS < 0
EV(2)
EF(3)
EV(3)
Distance (nanometers)

Figure 3b

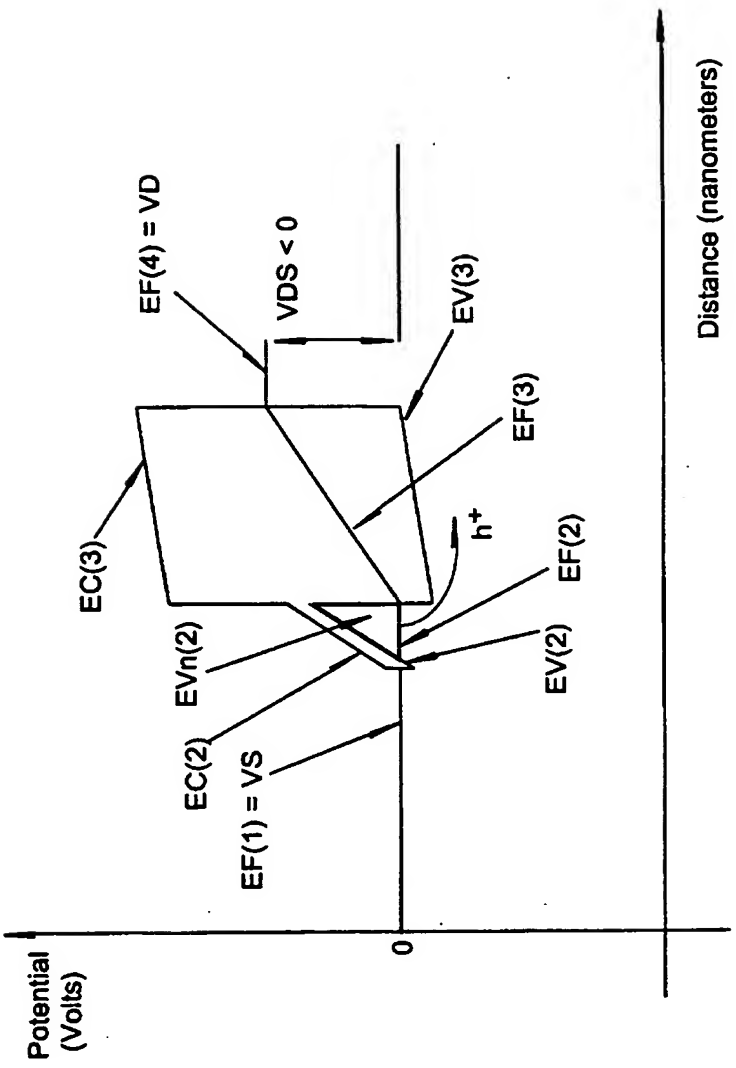

Potential (Volts)
Distance (nanometers)
0
EF(4) = VD
VDS < 0
EV(3)
EF(3)
EC(3)
h+
EF(2)
EV(2)
EVn(2)
EC(2)
EF(1) = VS

Figure 3c

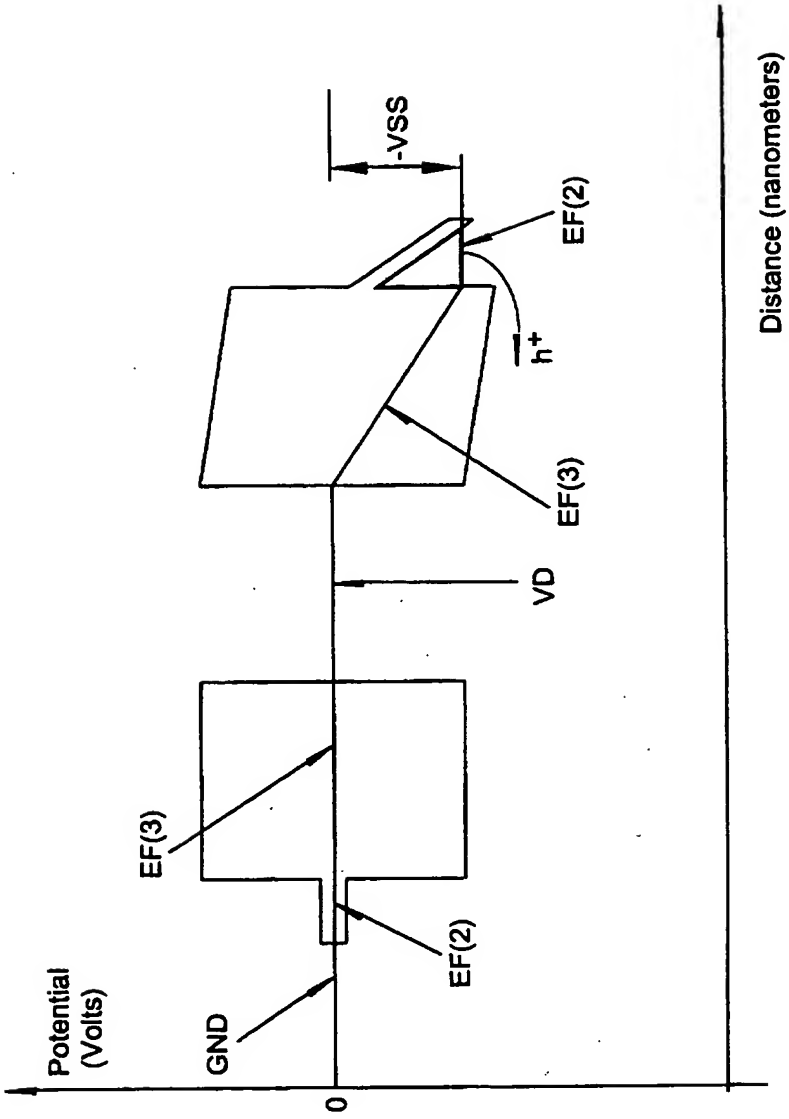

Potential (Volts)
Distance (nanometers)
GND
0
EF(3)
EF(2)
VD
EF(3)
h+
EF(2)
-VSS

Figure 4a

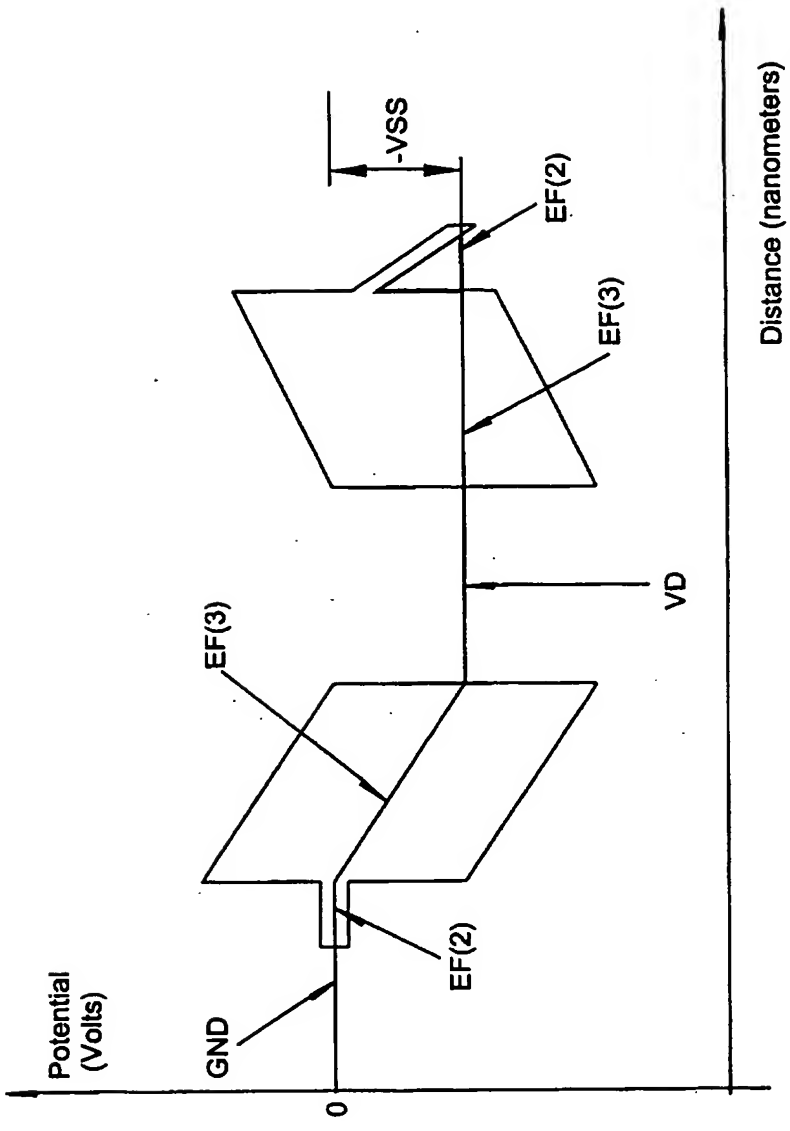

Potential (Volts)
GND
0
EF(2)
EF(3)
VD
-VSS
EF(2)
EF(3)
Distance (nanometers)

Figure 4b

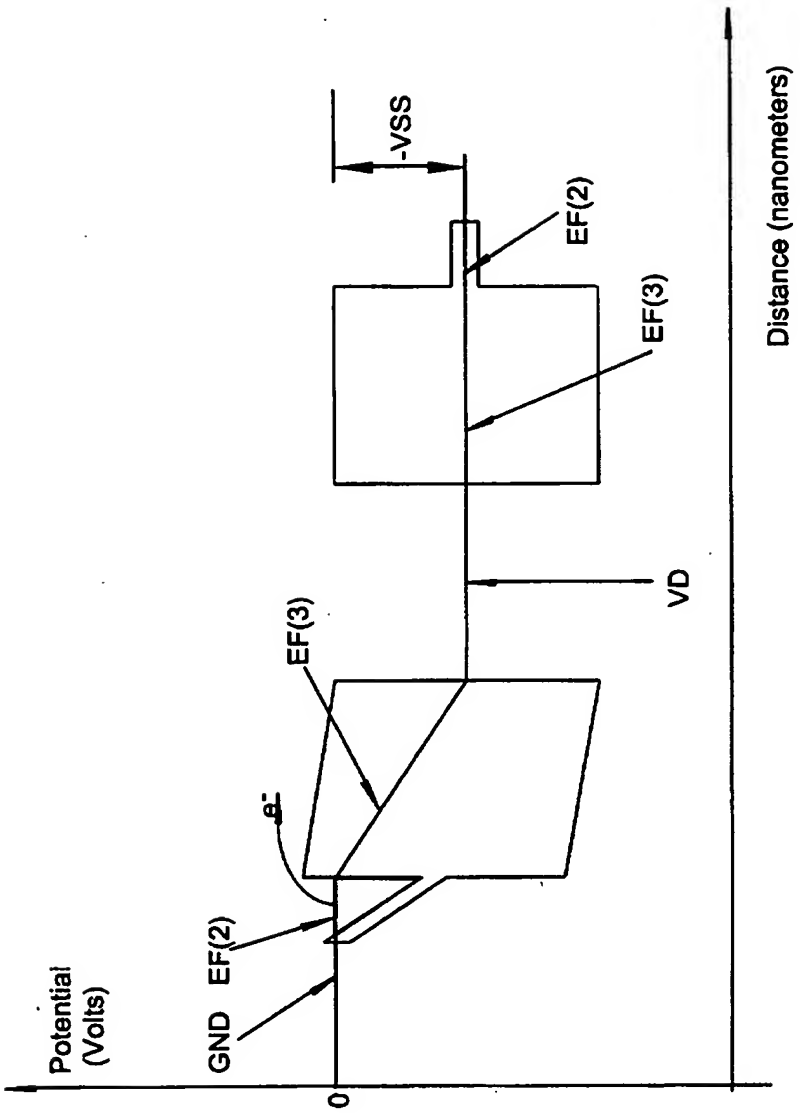

Potential (Volts)
Distance (nanometers)
0
GND
EF(2)
e⁻
EF(3)
VD
-VSS
EF(2)
EF(3)

Figure 4c

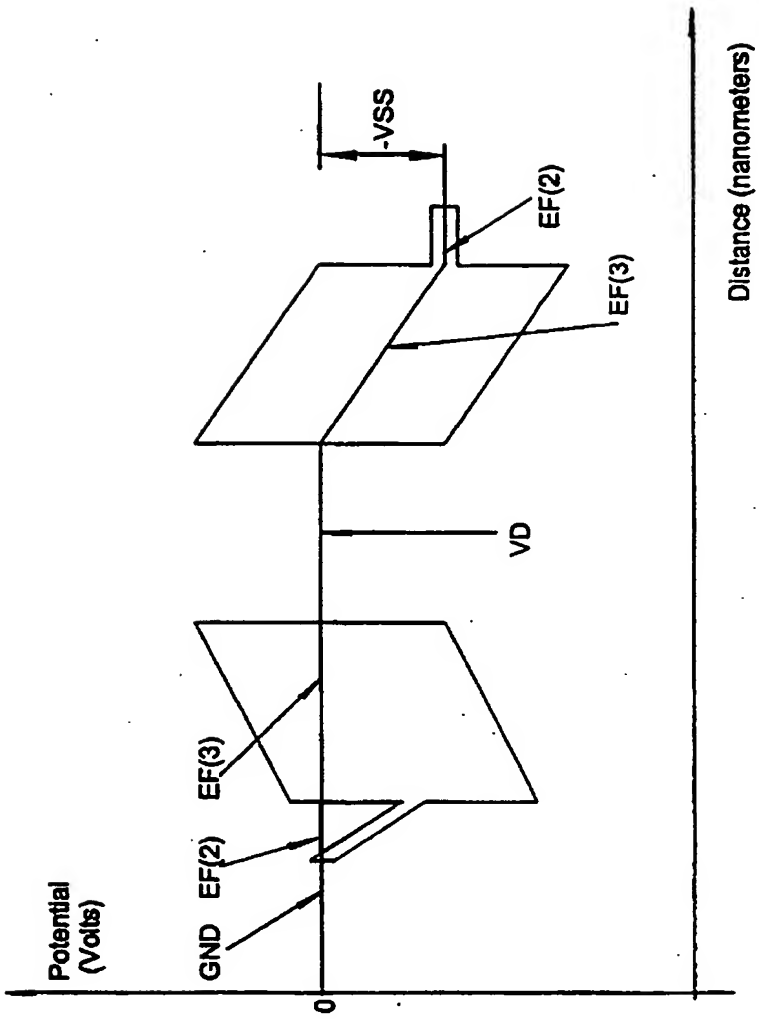

Potential (Volts)
GND
EF(2)
EF(3)
0
VD
-VSS
EF(2)
EF(3)
Distance (nanometers)

Figure 4d

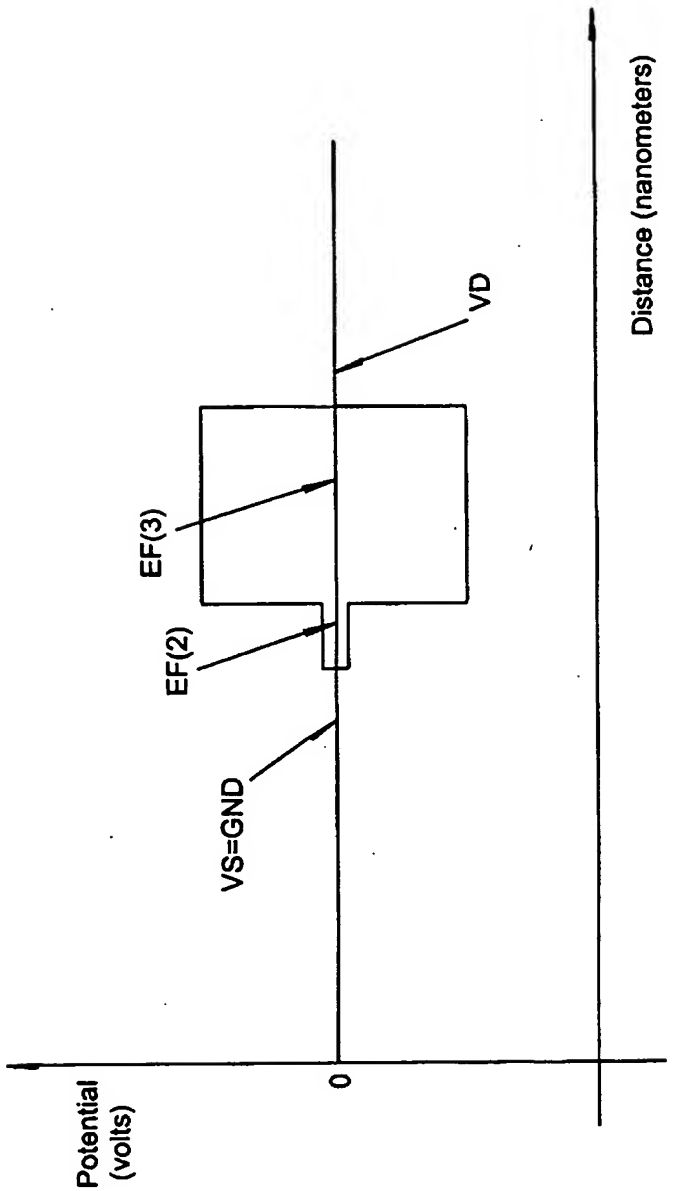


Figure 5a

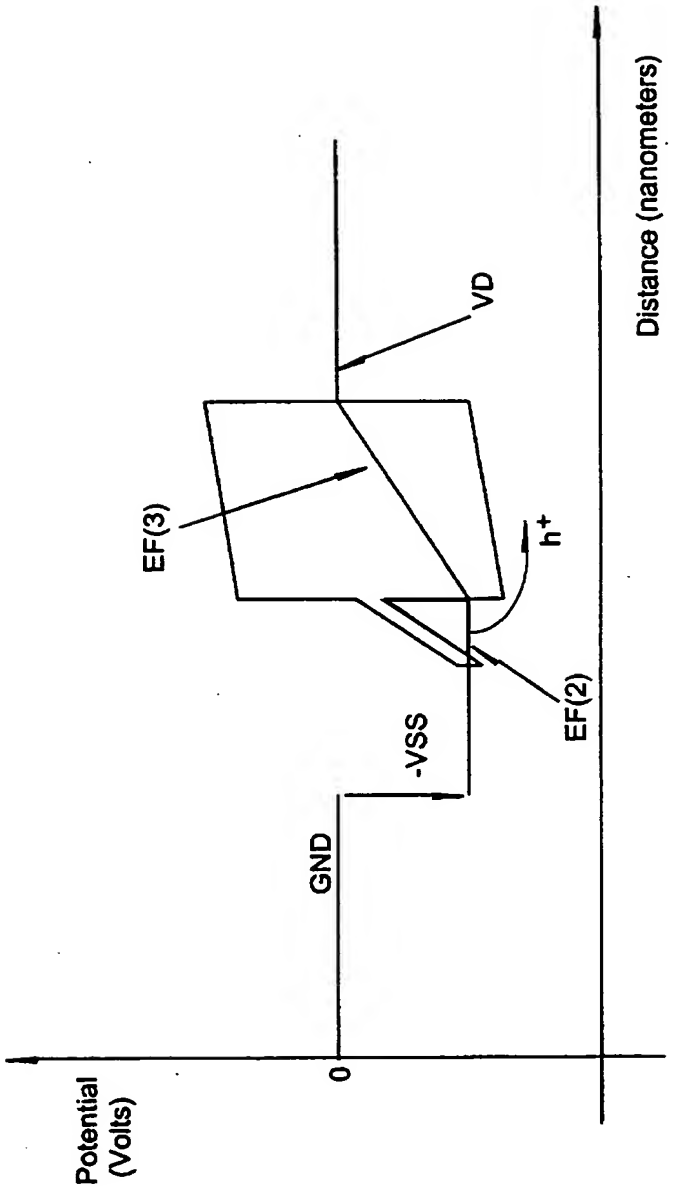


Figure 5b

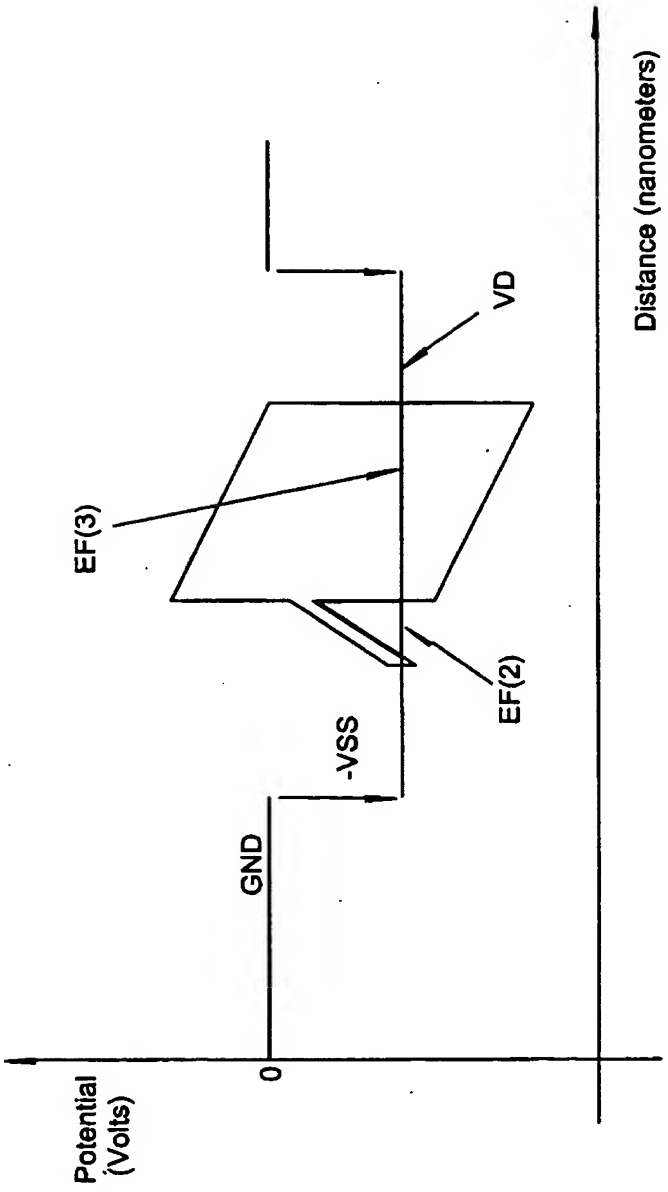


Figure 5c

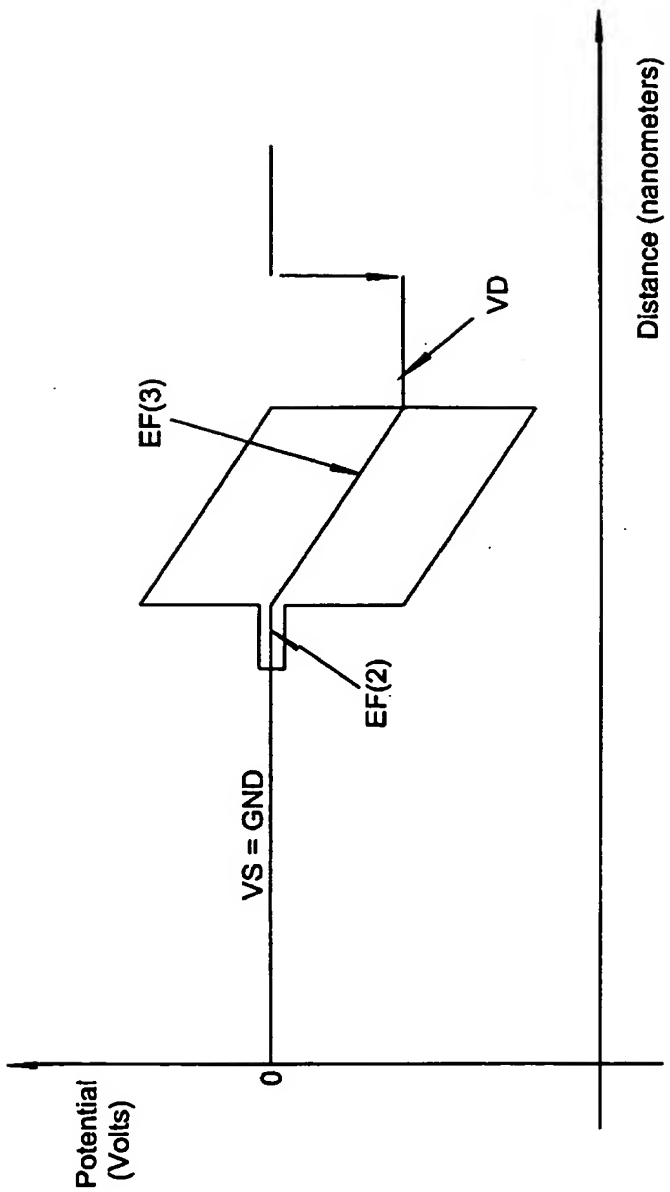


Figure 5d

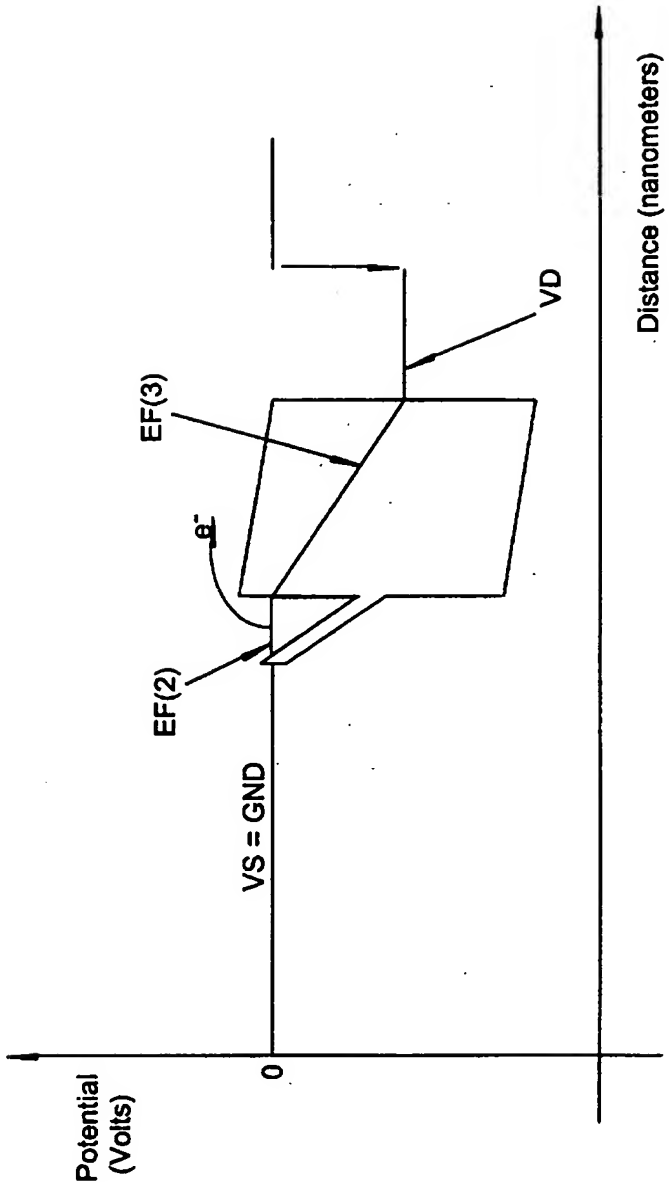


Figure 5e

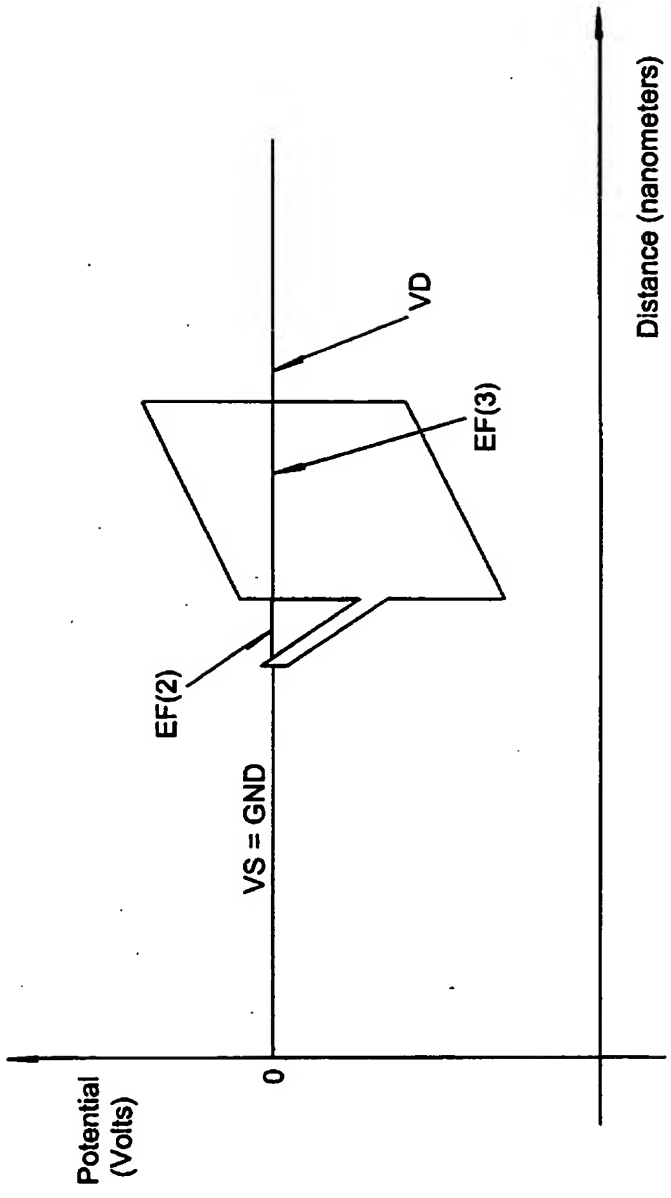


Figure 5f

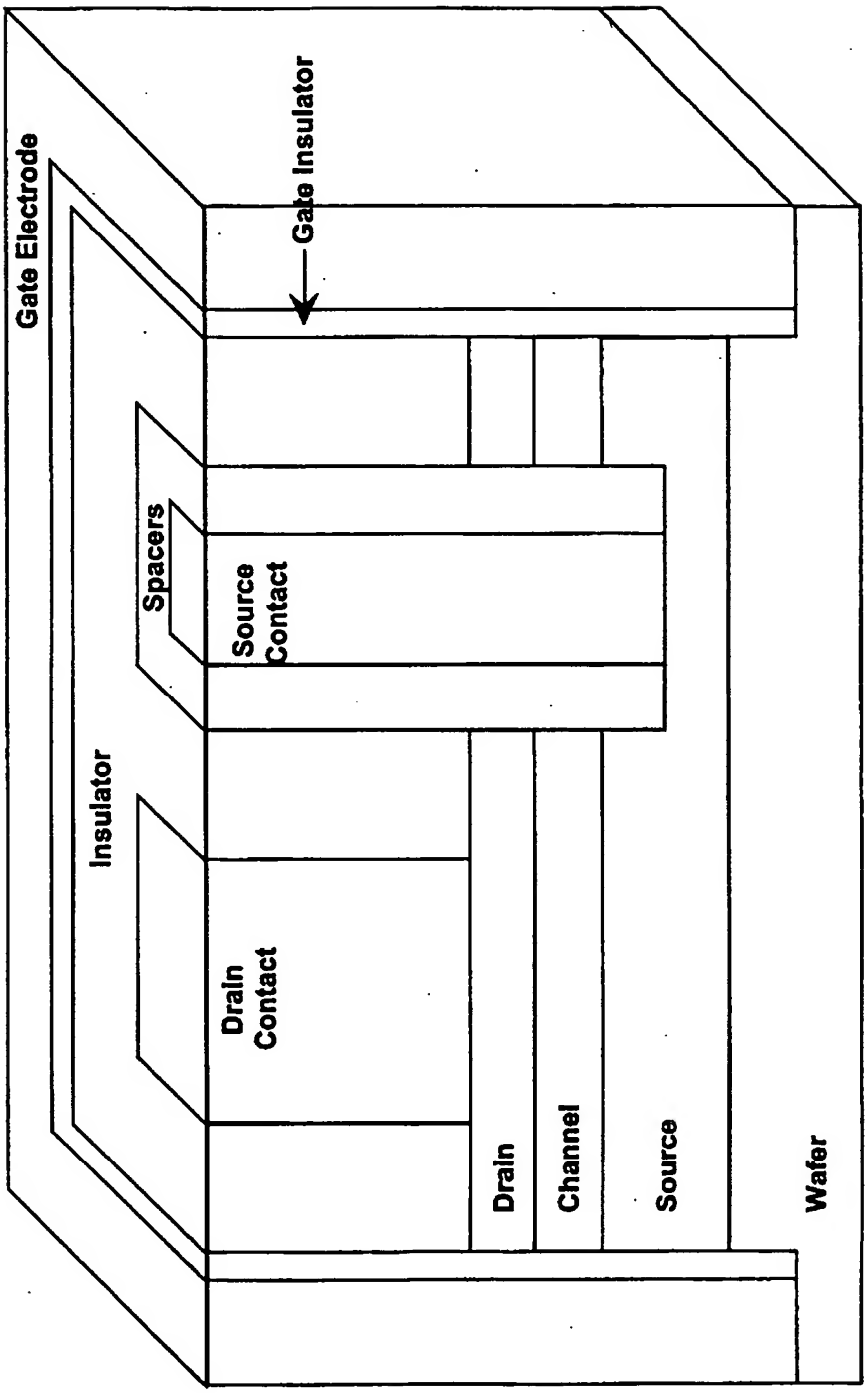

Gate Electrode
Gate Insulator
Spacers
Source Contact
Insulator
Drain Contact
Drain
Channel
Source
Wafer

Figure 6

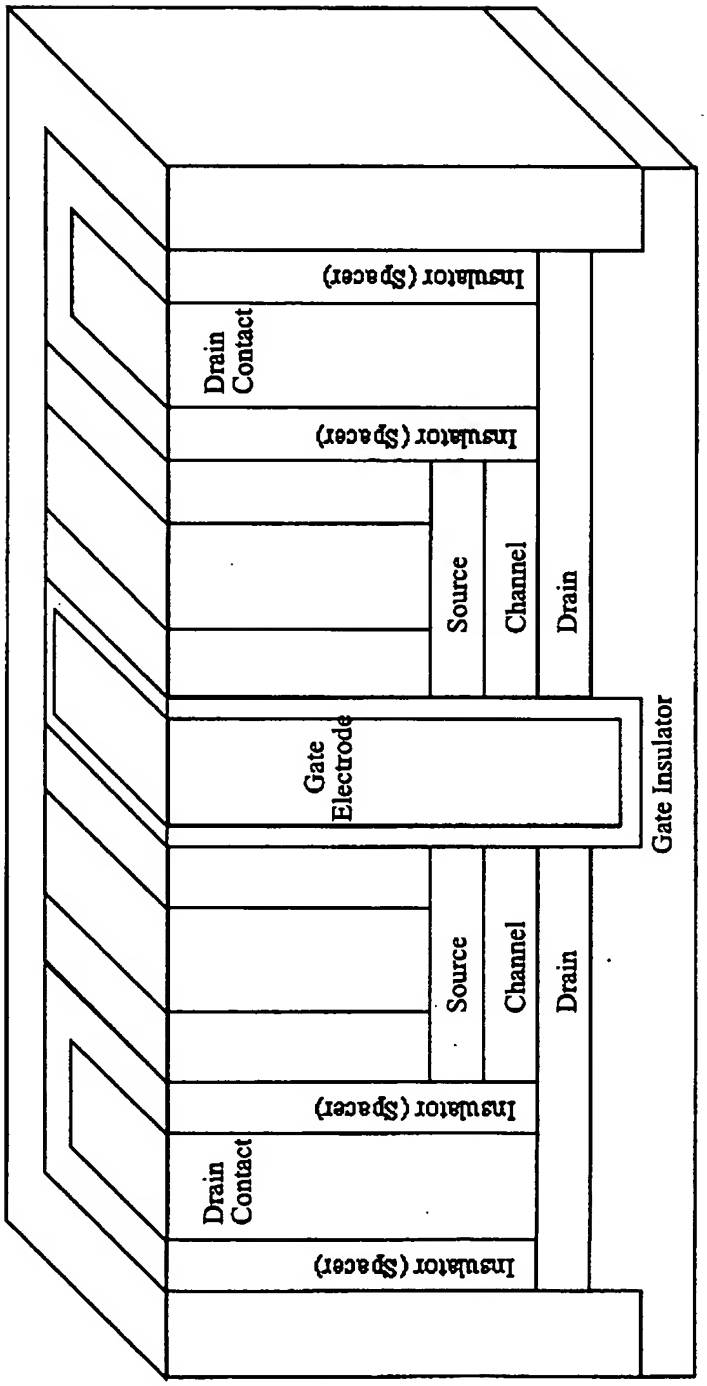

Insulator (Spacer)
Drain Contact
Insulator (Spacer)
Source
Channel
Drain
Gate Electrode
Gate Insulator
Source
Channel
Drain
Insulator (Spacer)
Drain Contact
Insulator (Spacer)

Figure 7a

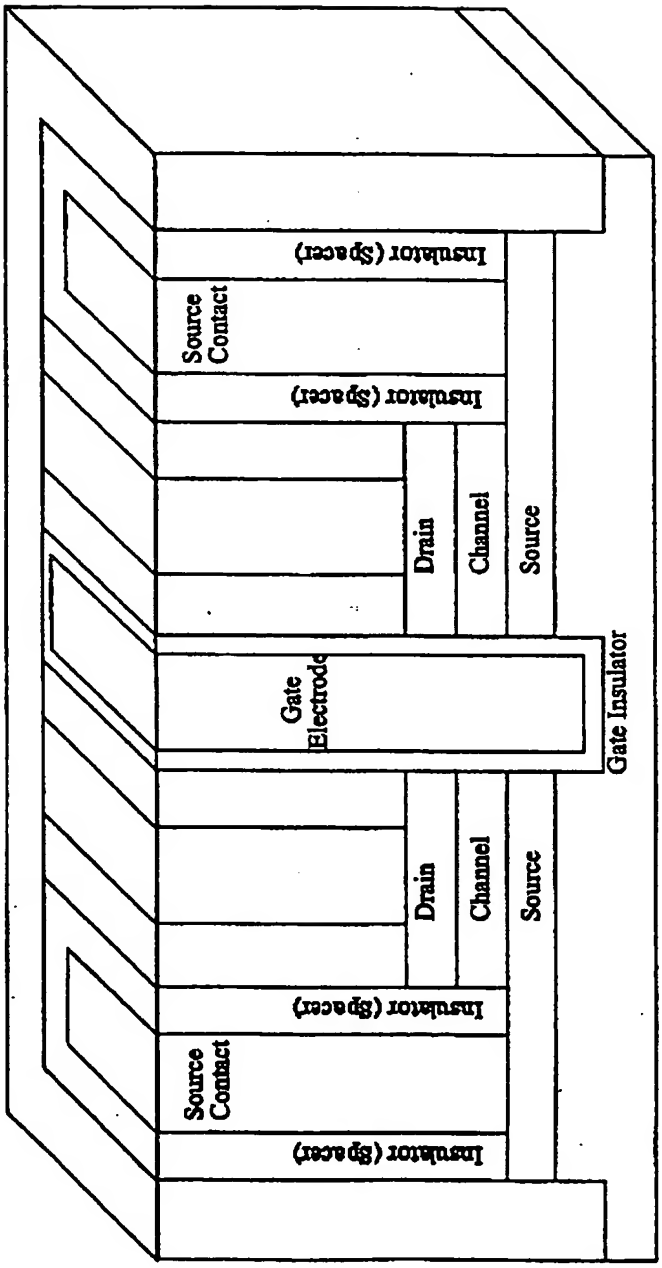

Insulator (Spacer)
Source Contact
Insulator (Spacer)
Drain
Channel
Source
Gate Electrode
Gate Insulator
Drain
Channel
Source
Insulator (Spacer)
Source Contact
Insulator (Spacer)

Figure 7b

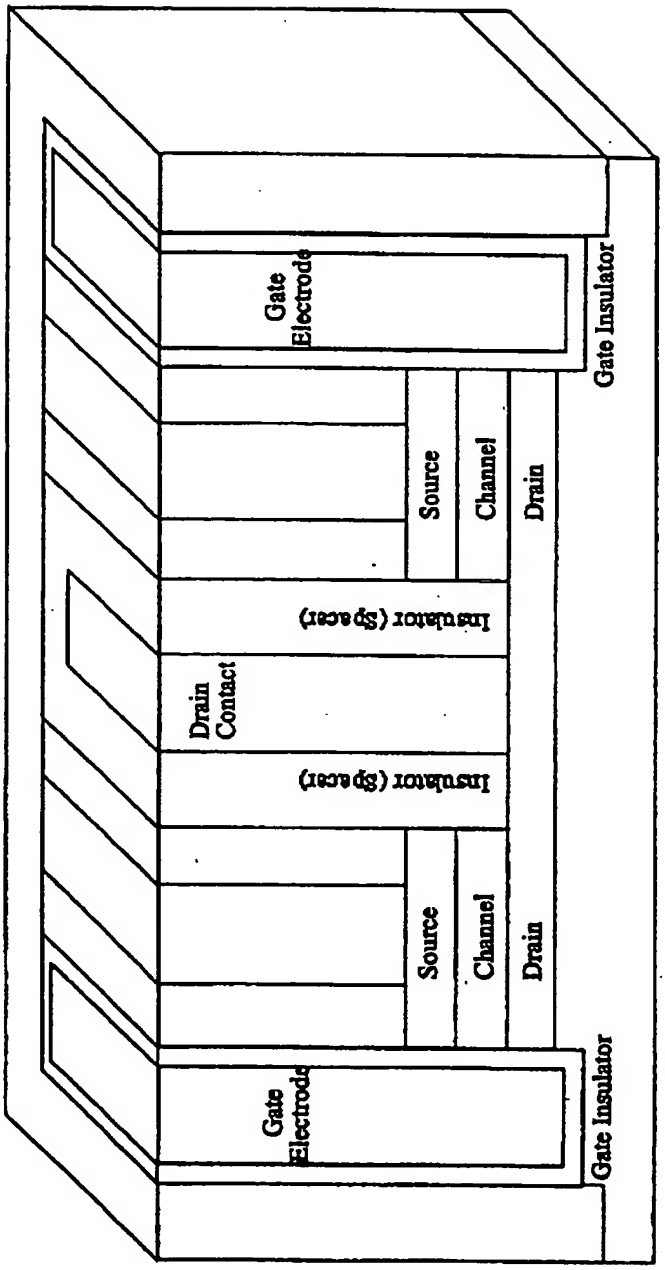

Gate Electrode
Gate Insulator
Source
Channel
Drain
Insulator (Spacer)
Drain Contact
Insulator (Spacer)
Source
Channel
Drain
Gate Electrode
Gate Insulator

Figure 7c

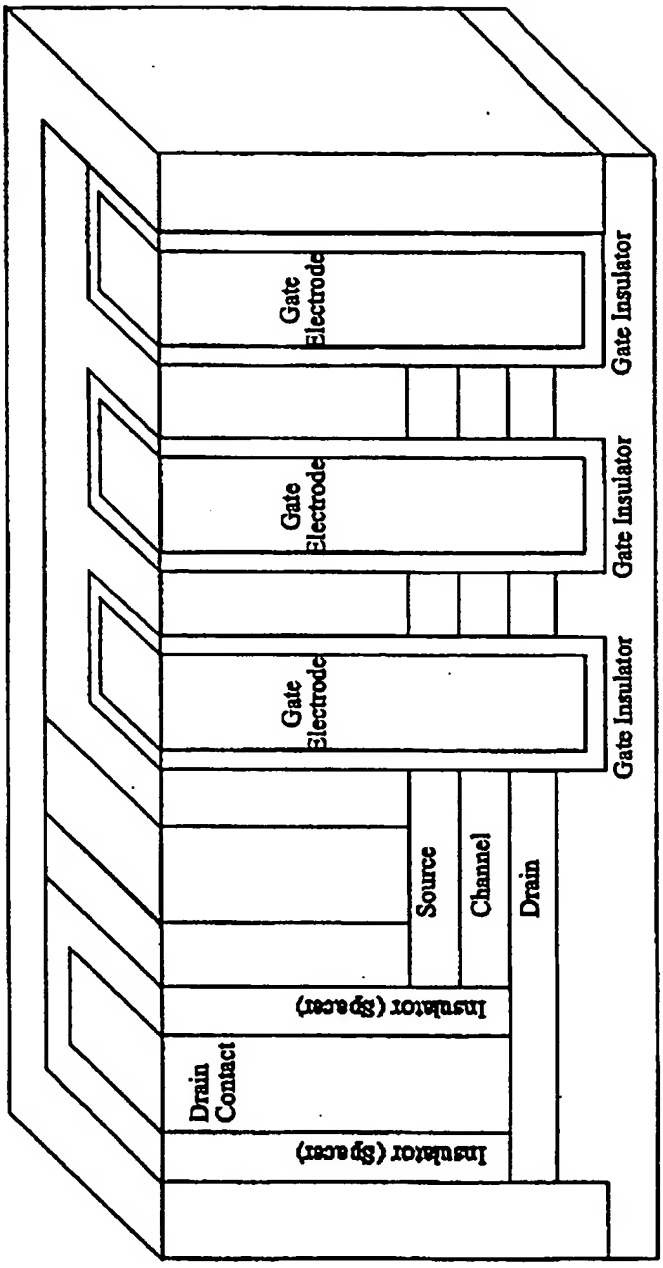
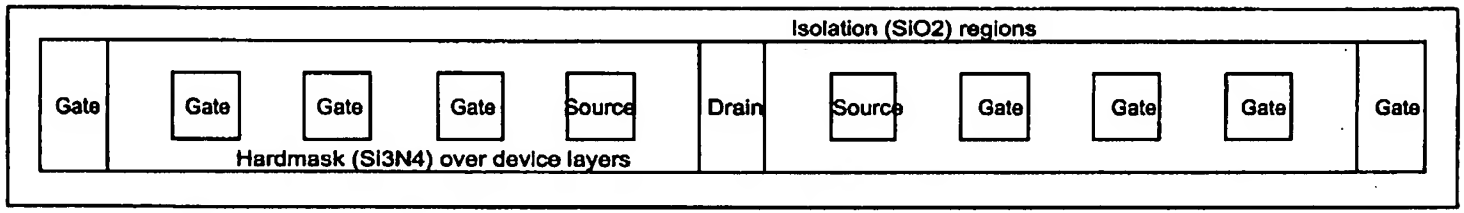

Gate Electrode
Gate Insulator
Gate Electrode
Gate Insulator
Gate Electrode
Gate Insulator
Source
Channel
Drain
Insulator (Spacer)
Drain Contact
Insulator (Spacer)

Figure 8

Figure 9: 4-Input CMOS "NOR" Logic Gates



Figur 9a:
Static Source Voltage Supply (separate "NMOS" and "PMOS"

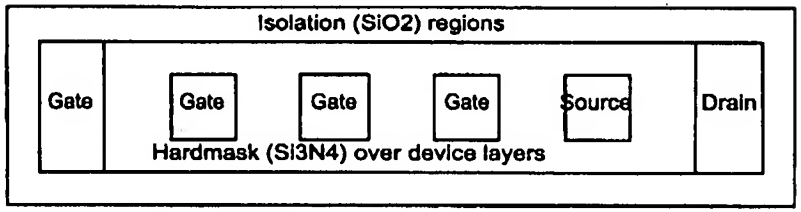


Figure 9b:
Dynamic Source Voltage Supply (single device as "NMOS" and "PMOS")

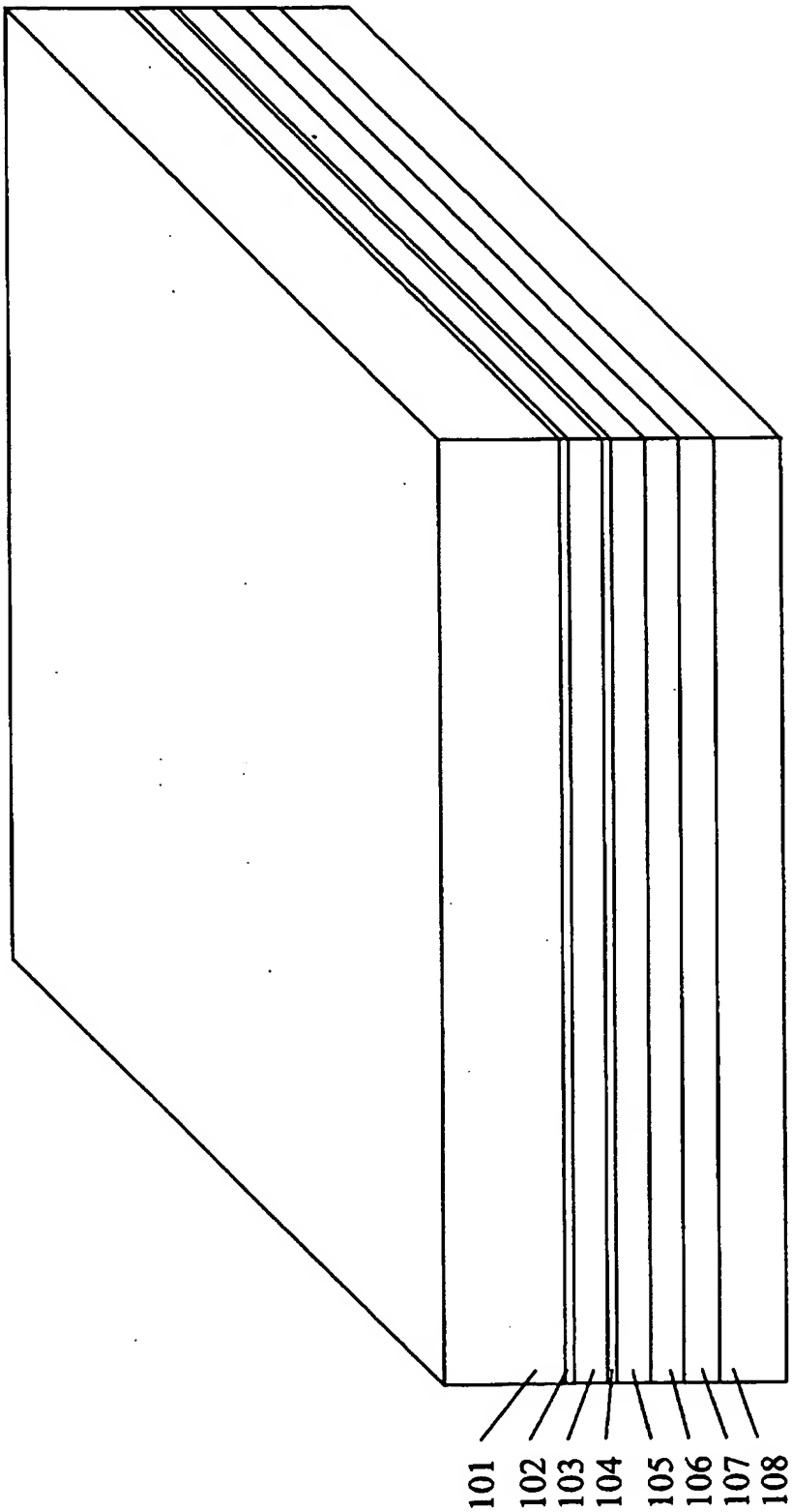


Figure 10A

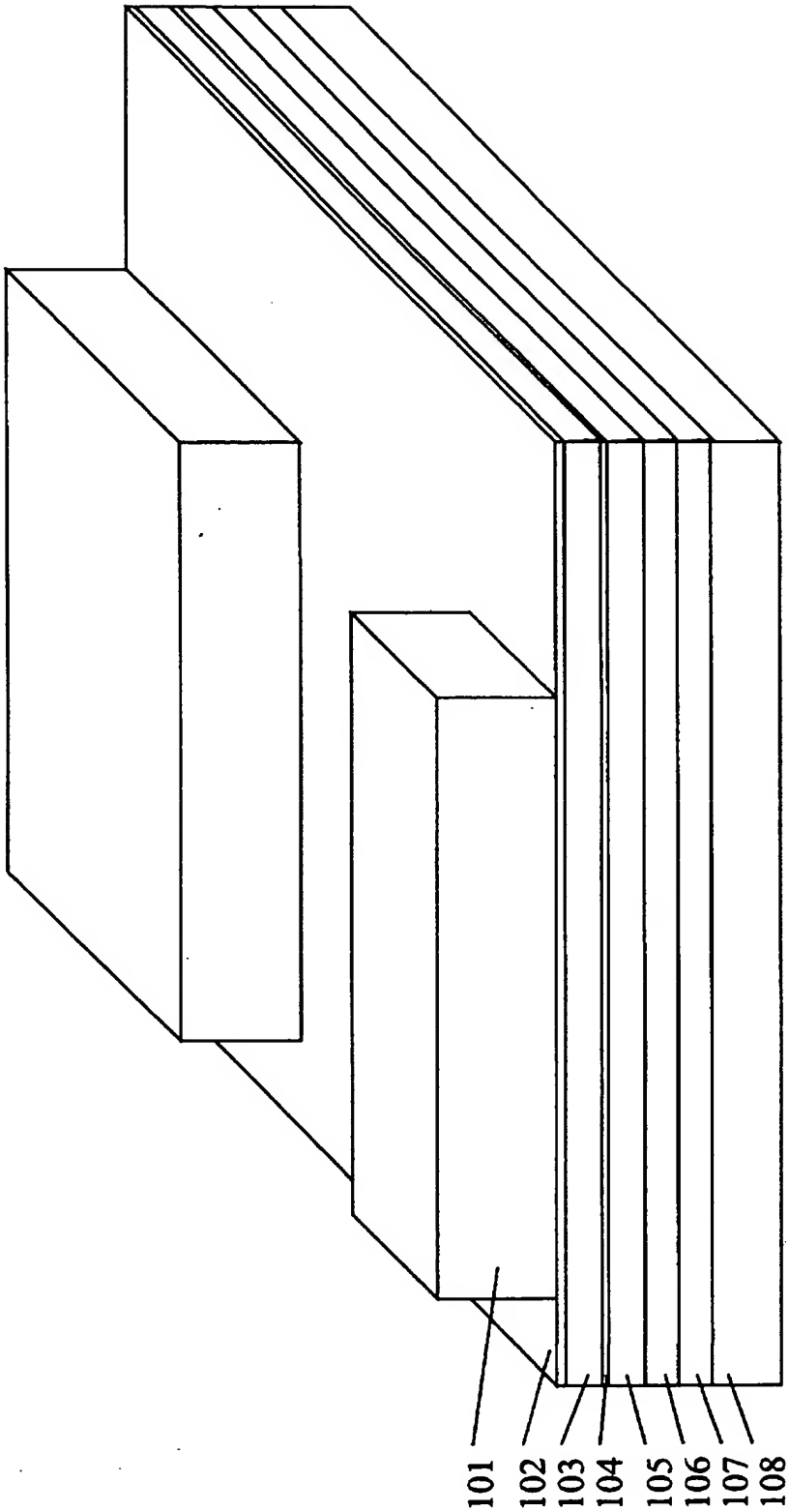


Figure 10B

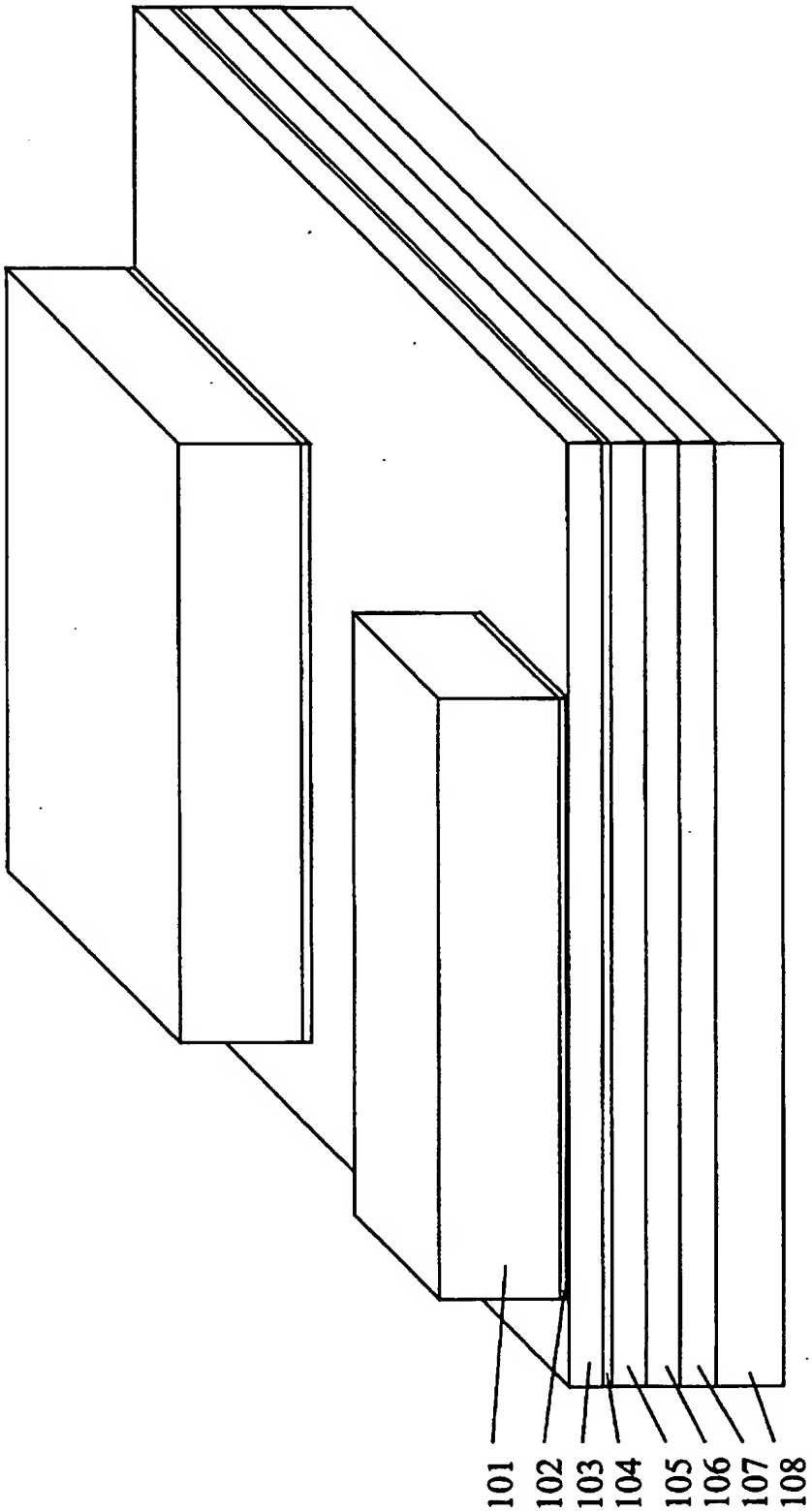


Figure 10C

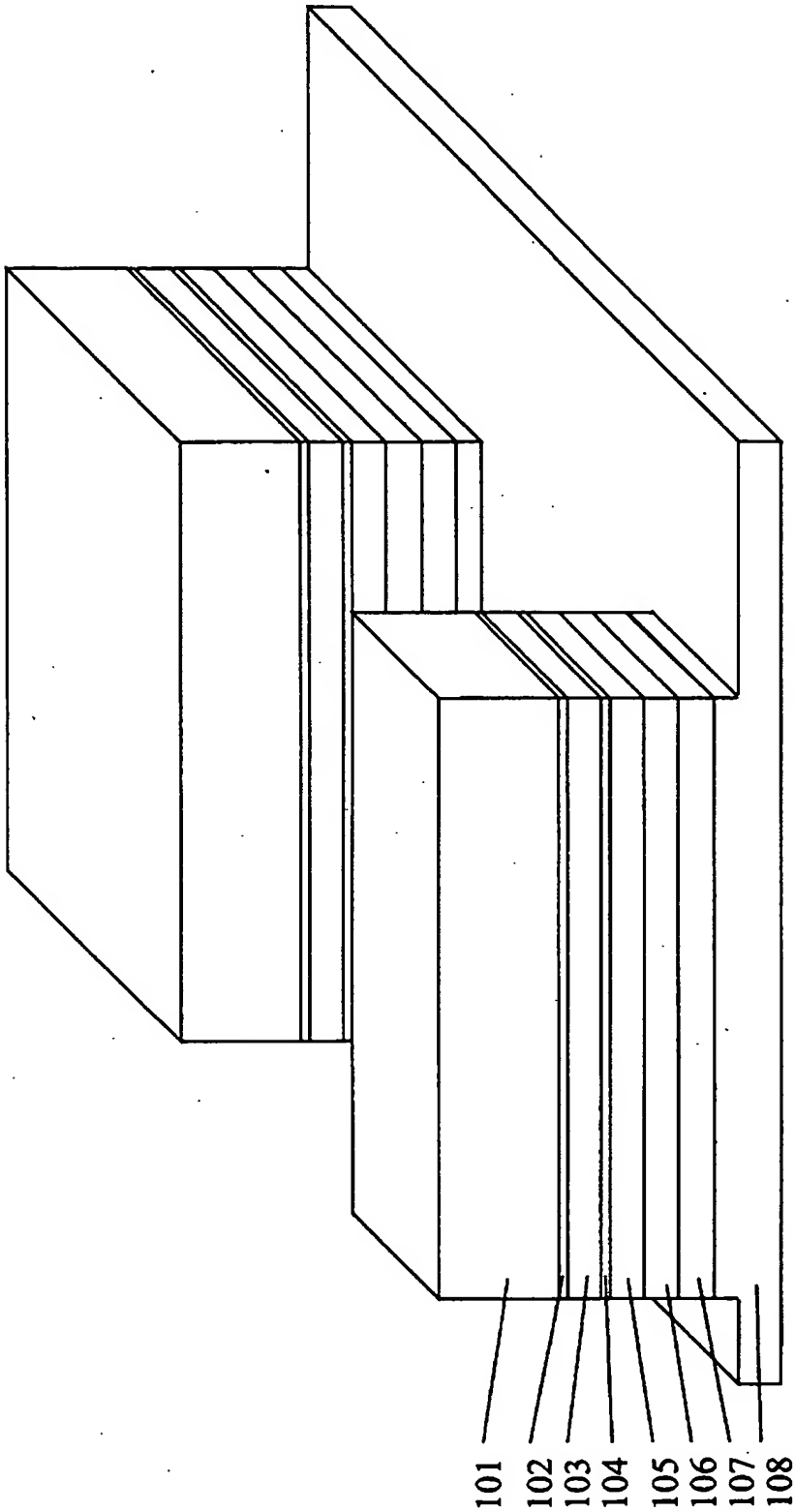


Figure 10D

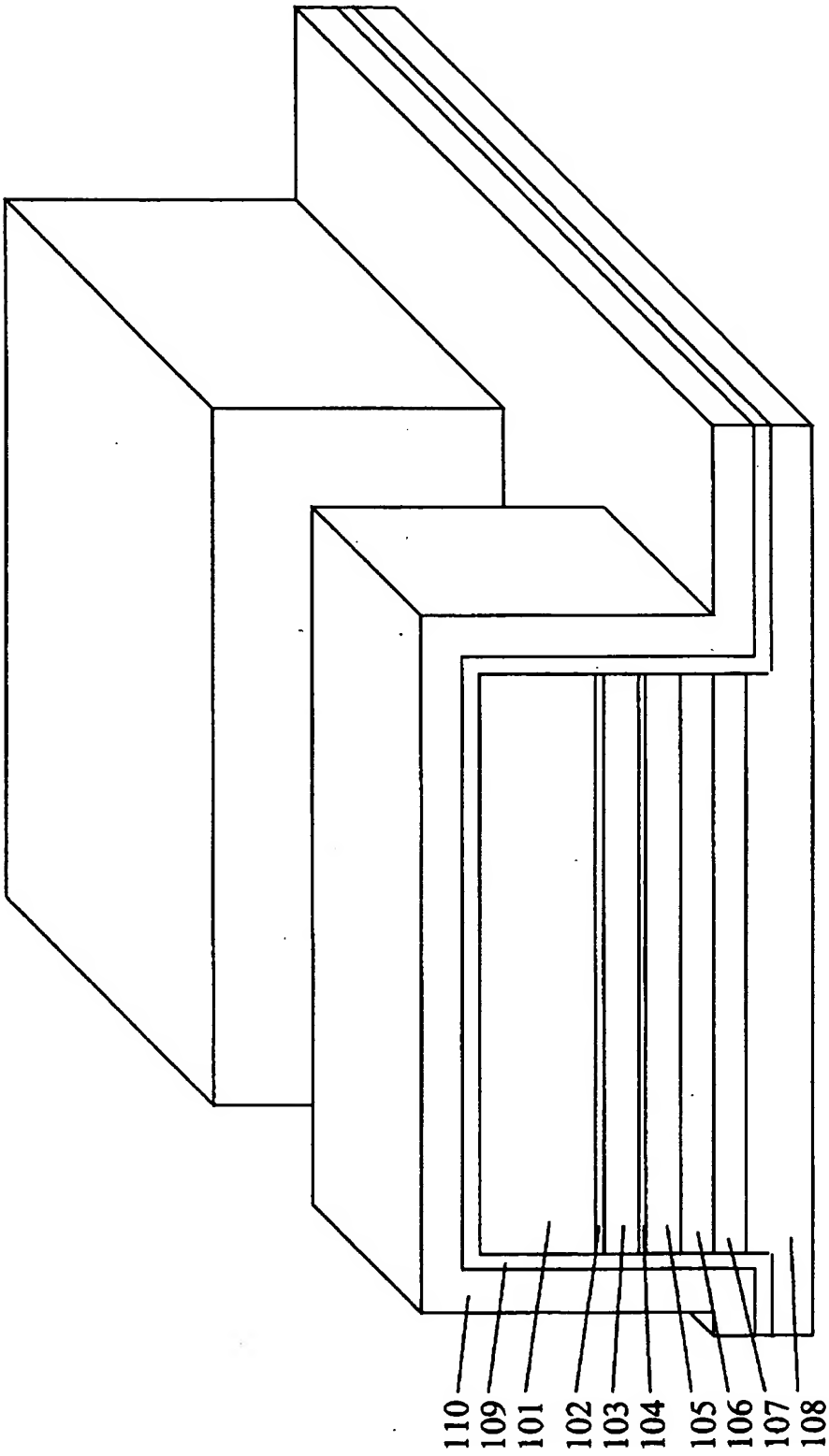


Figure 10E

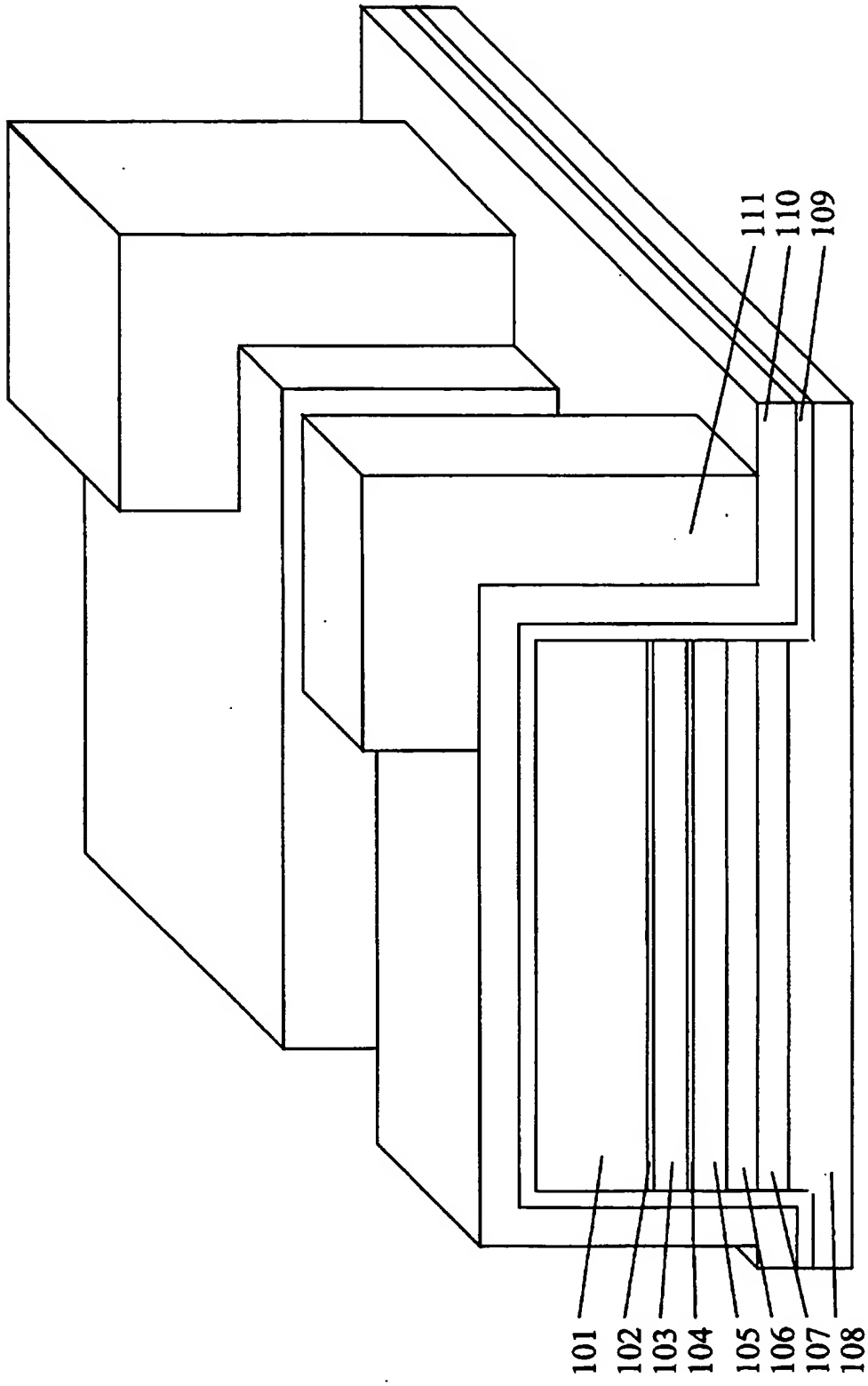


Figure 10F

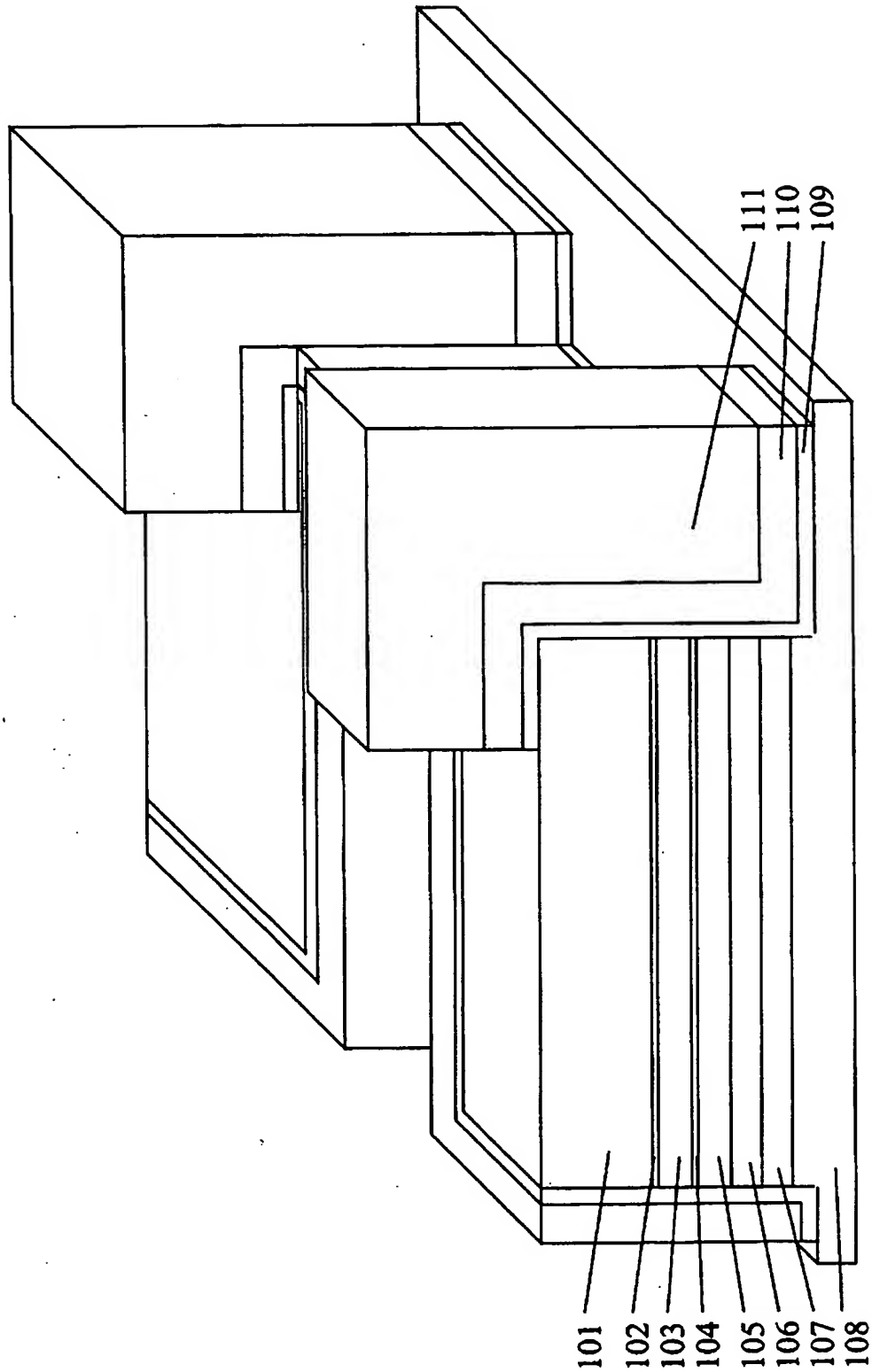


Figure 10G

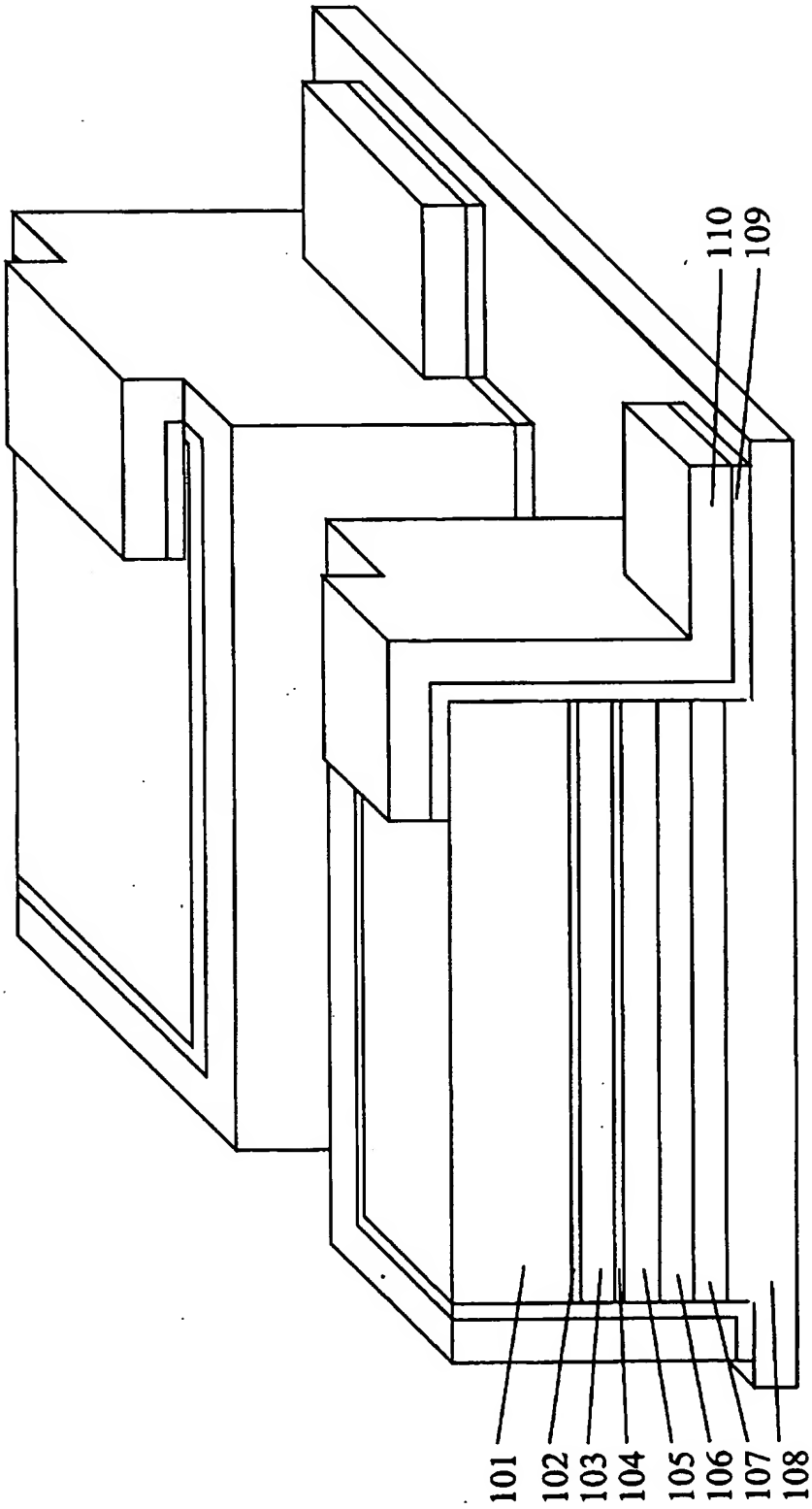


Figure 10H

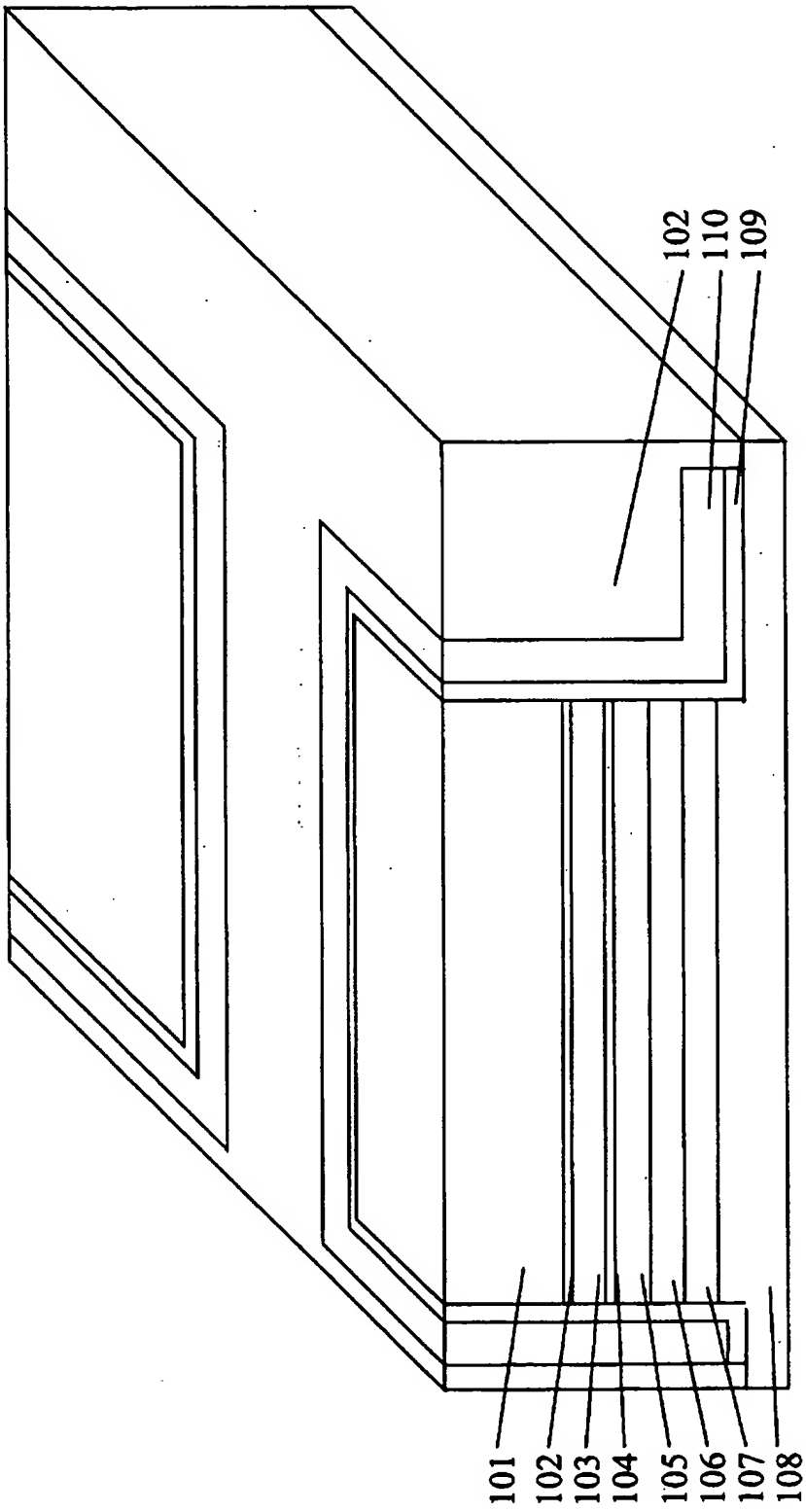


Figure 10I

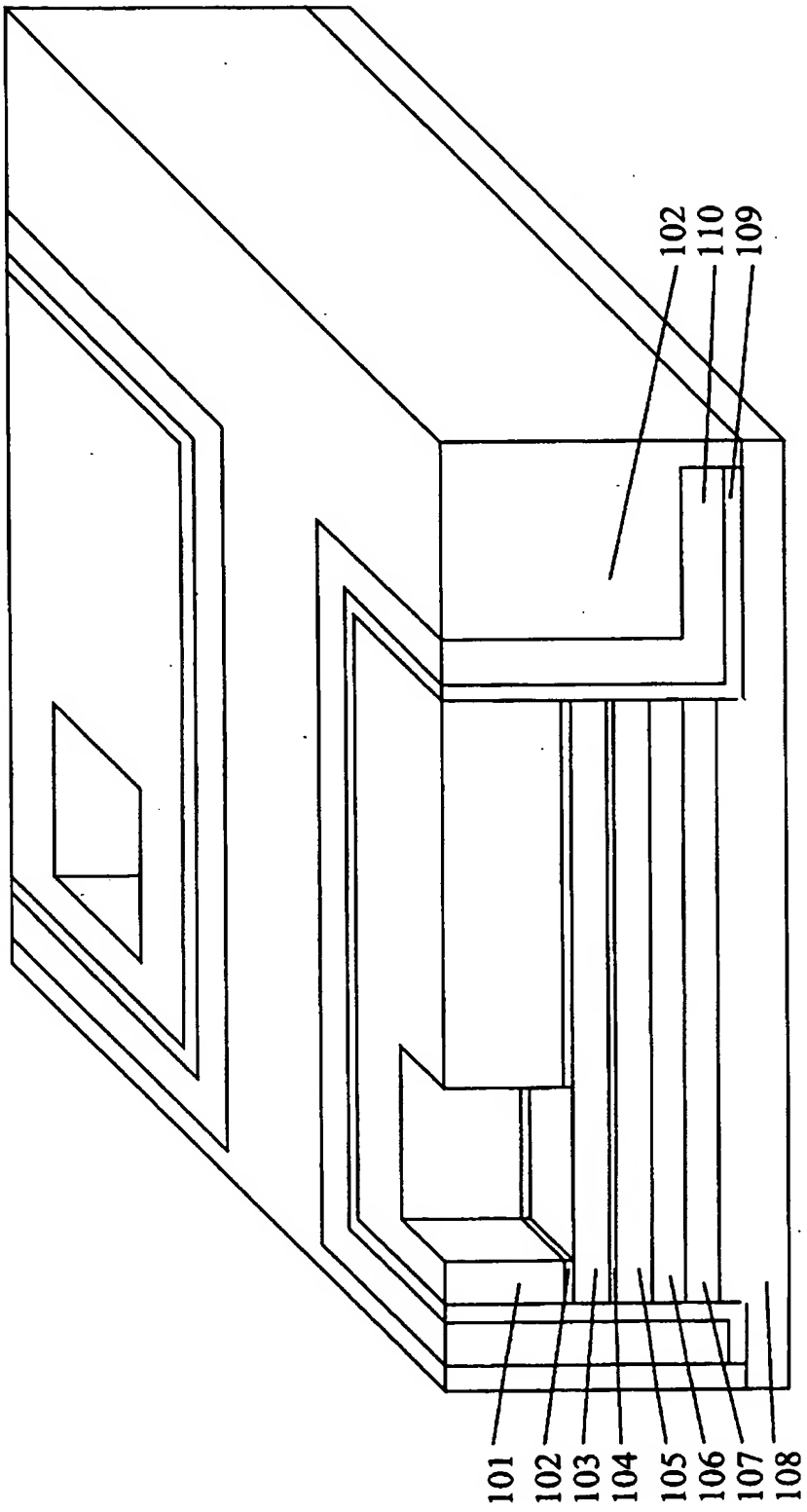


Figure 10J

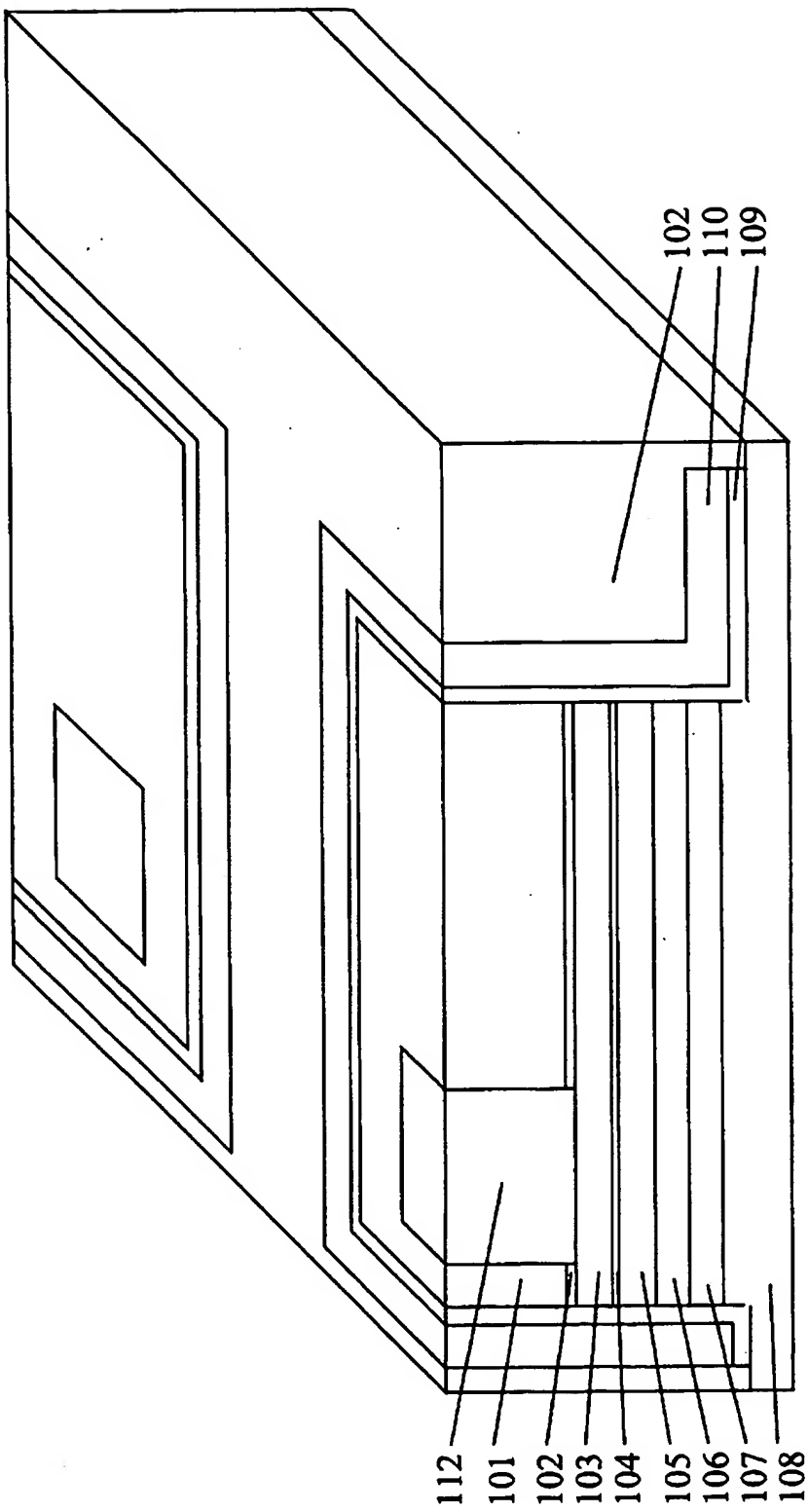


Figure 10K

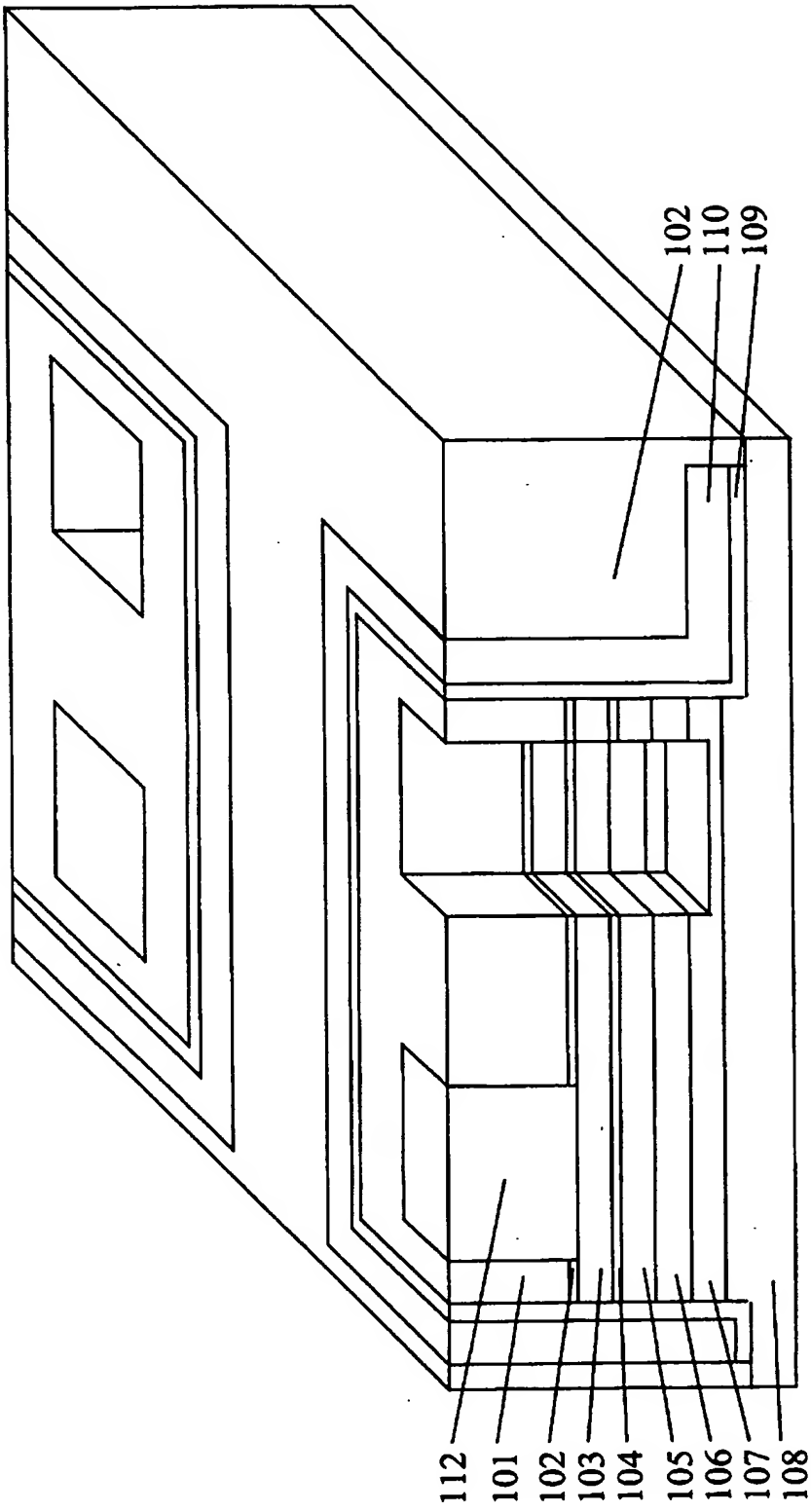


Figure 10L

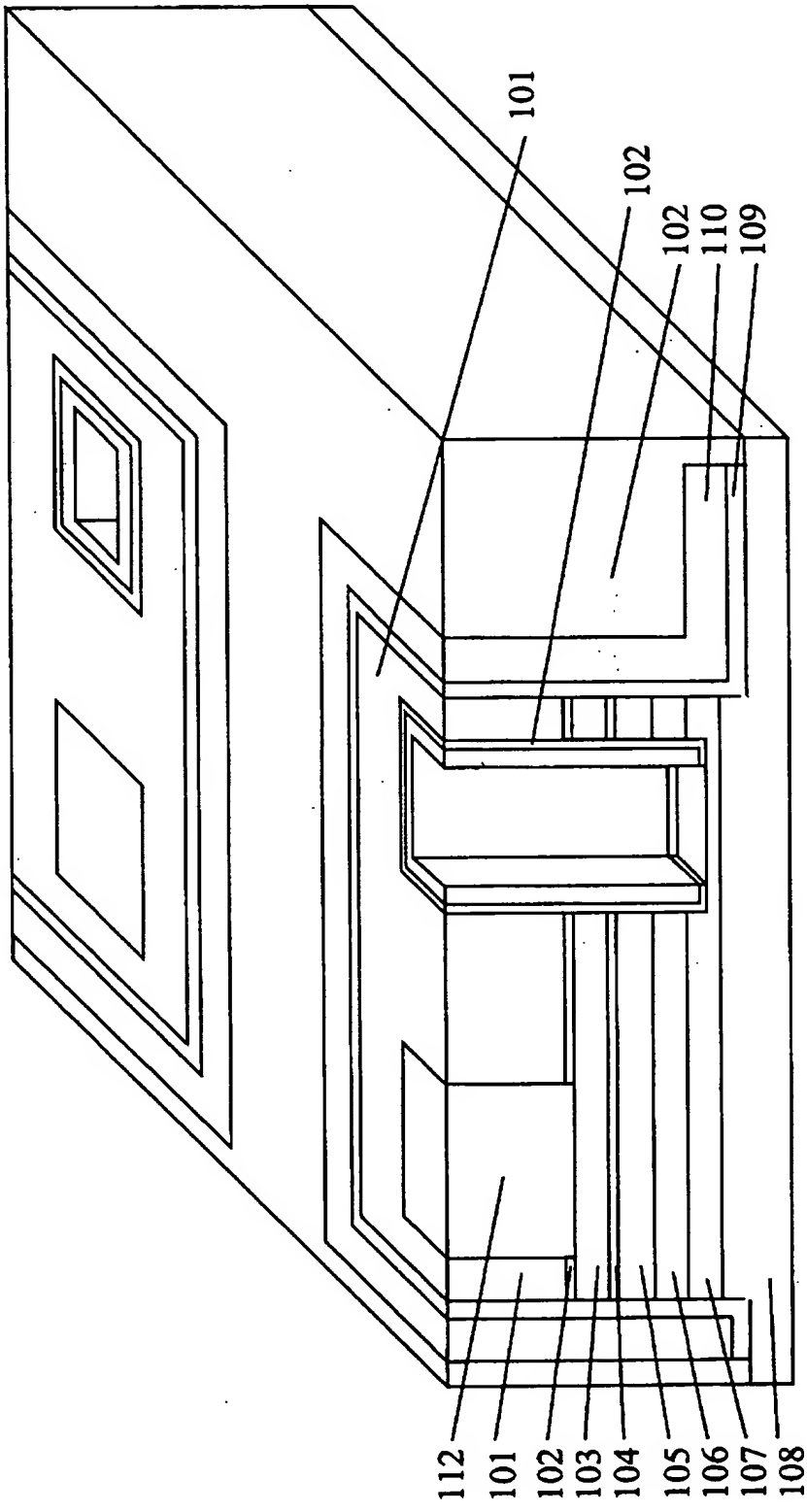


Figure 10M

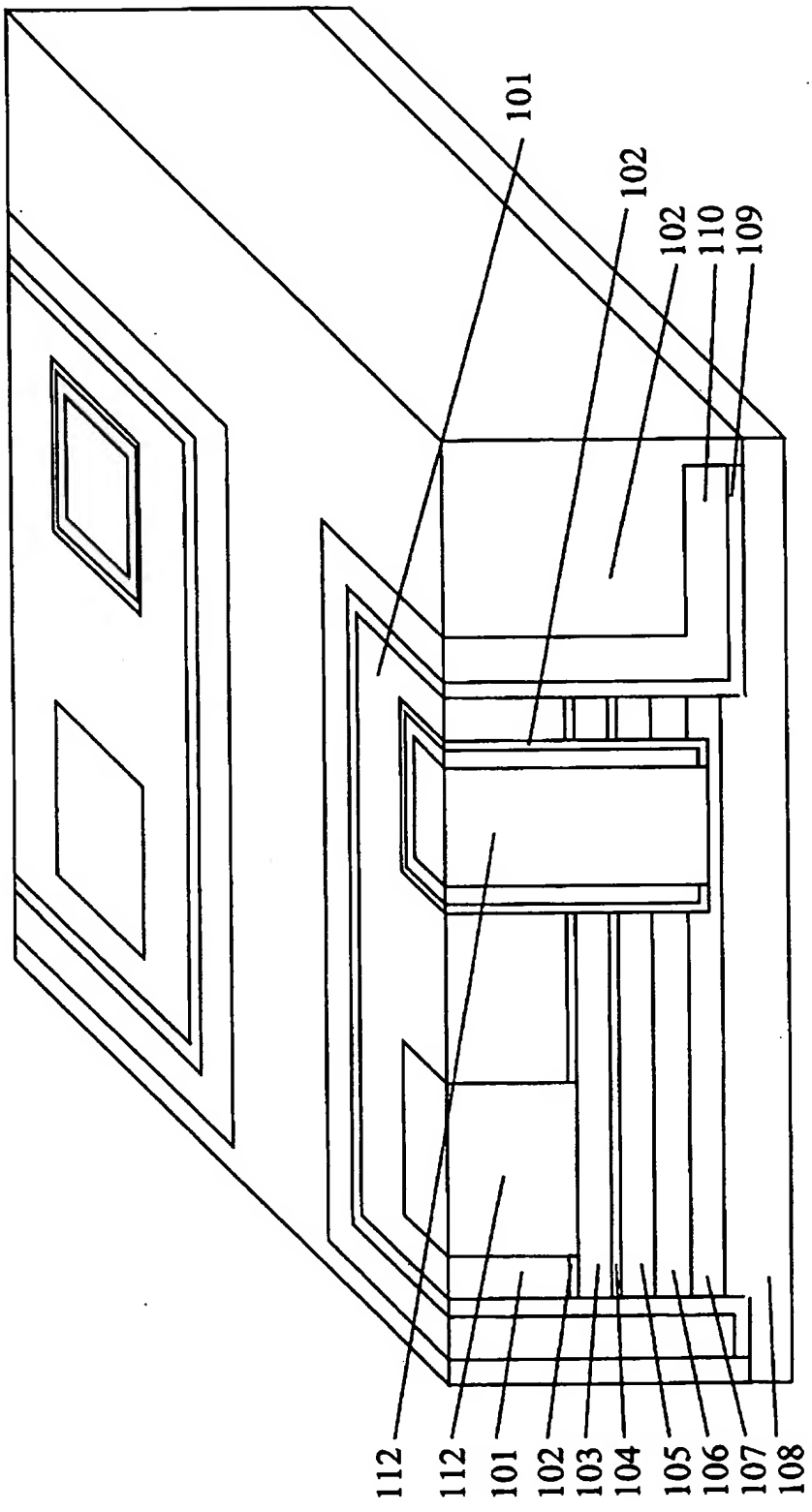


Figure 10N

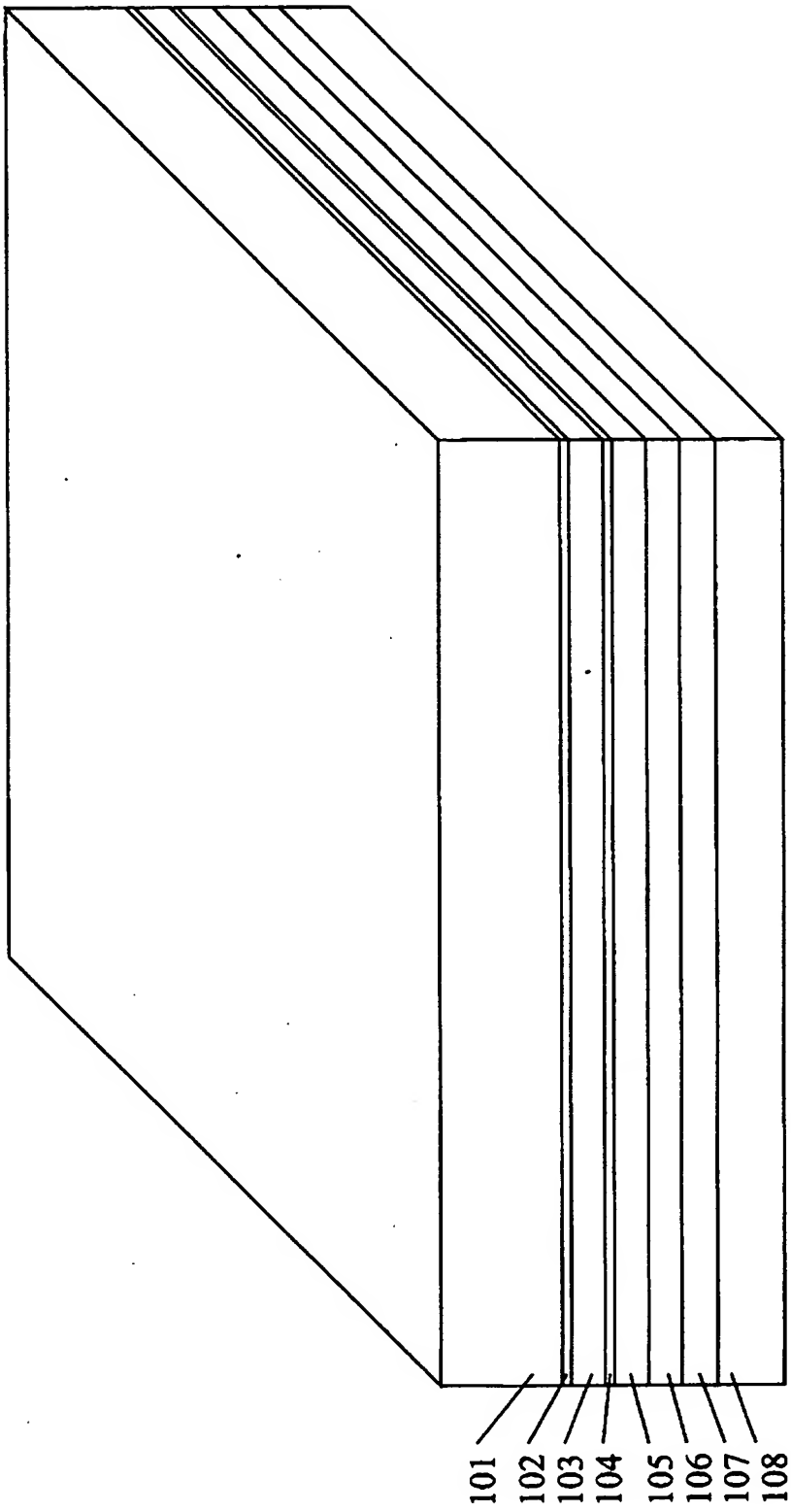


Figure 11A

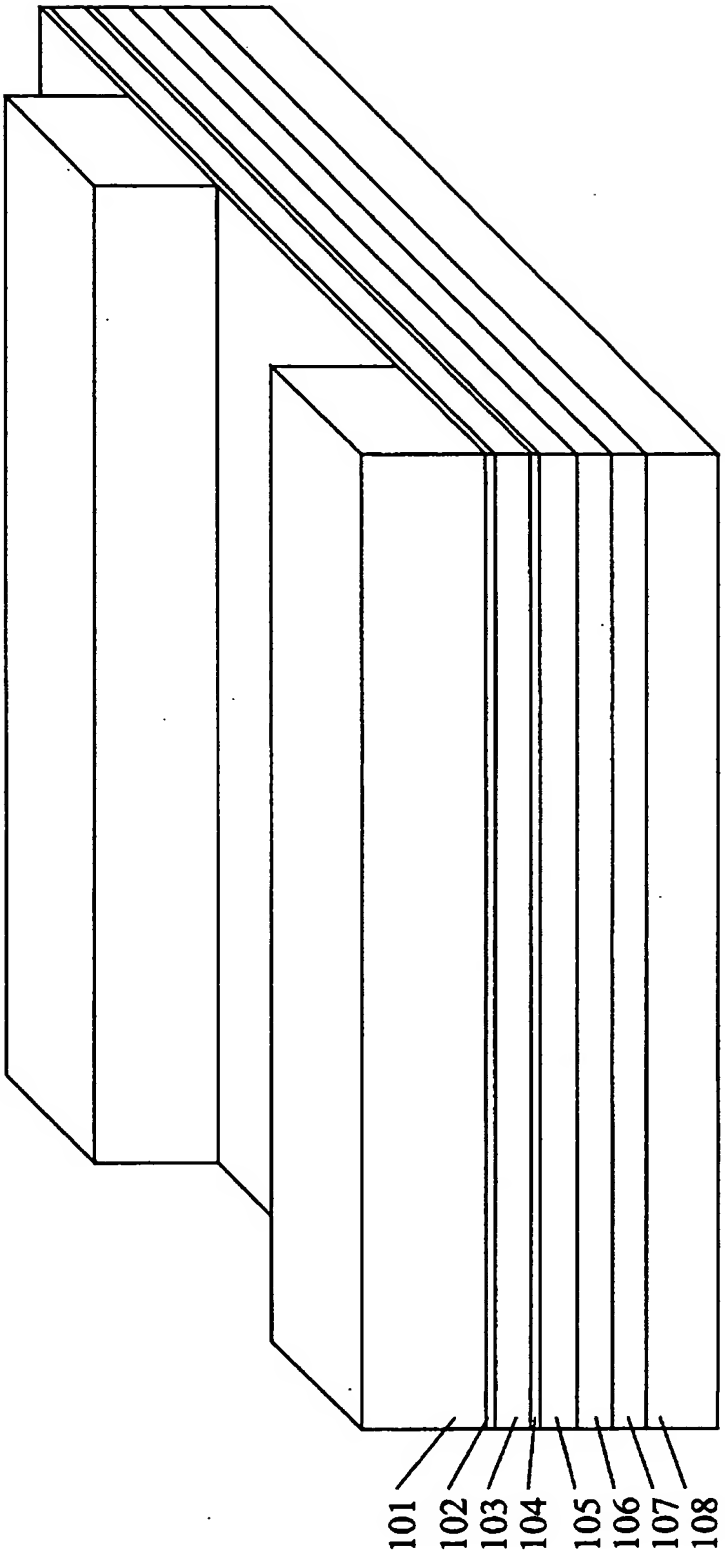


Figure 11B

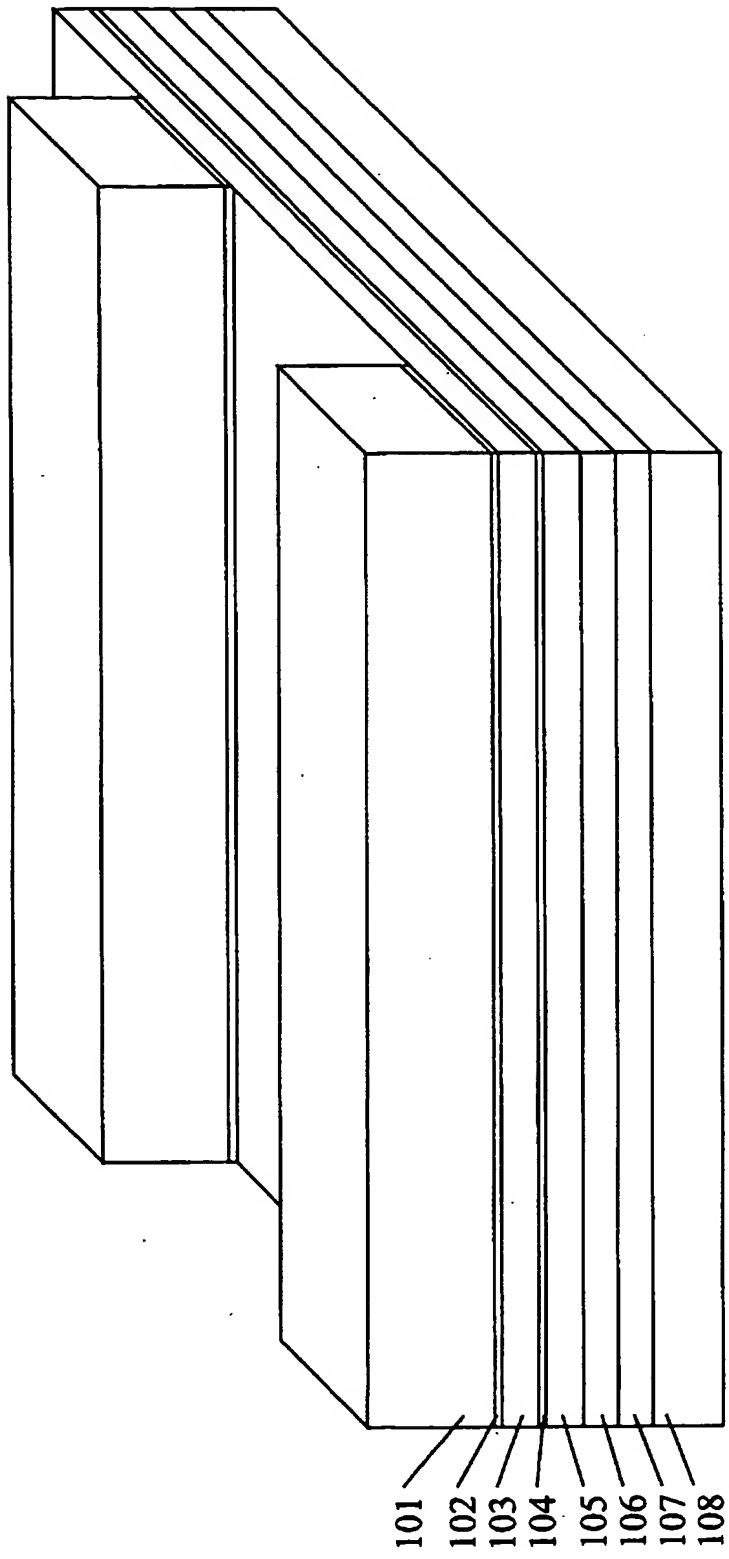


Figure 11C

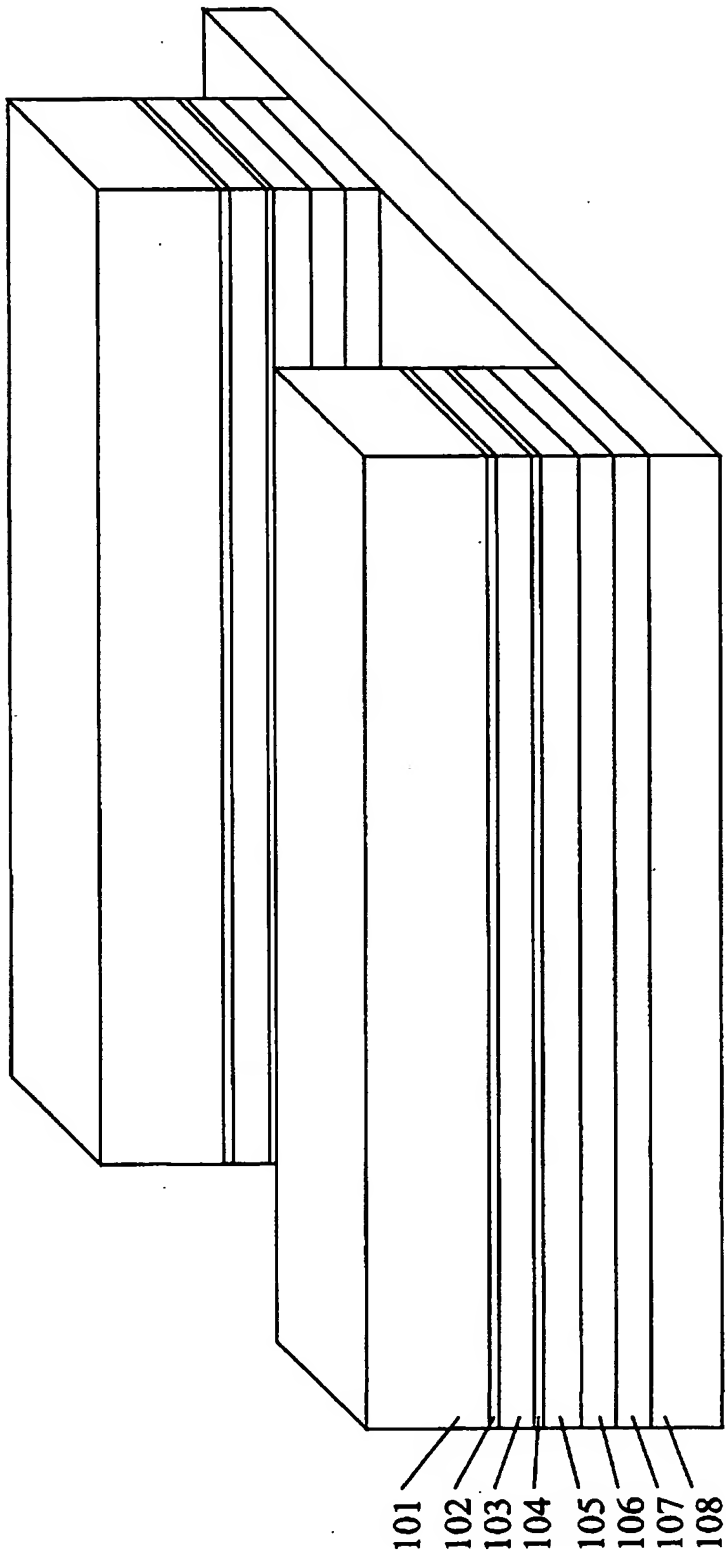


Figure 11D

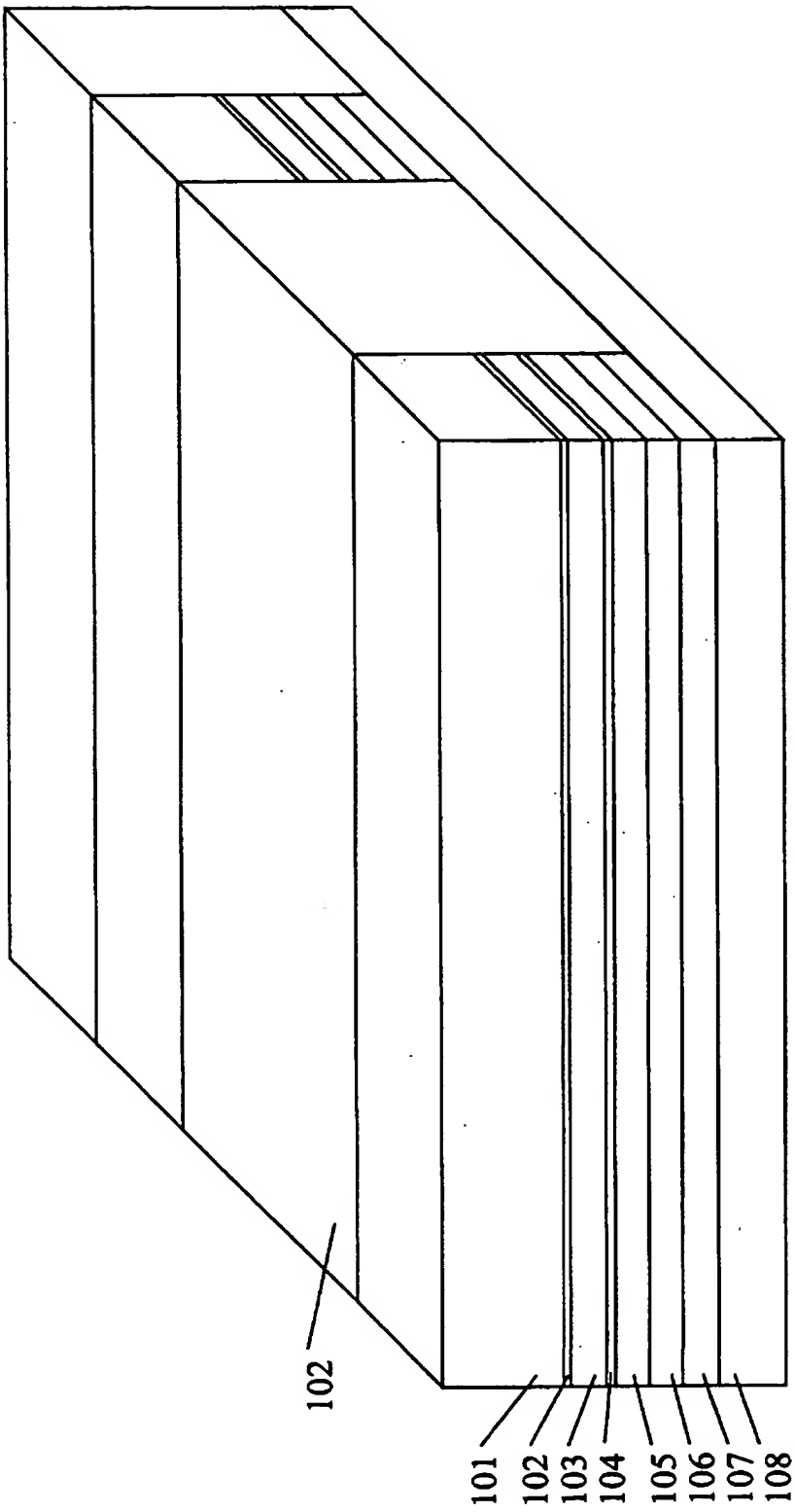


Figure 11E

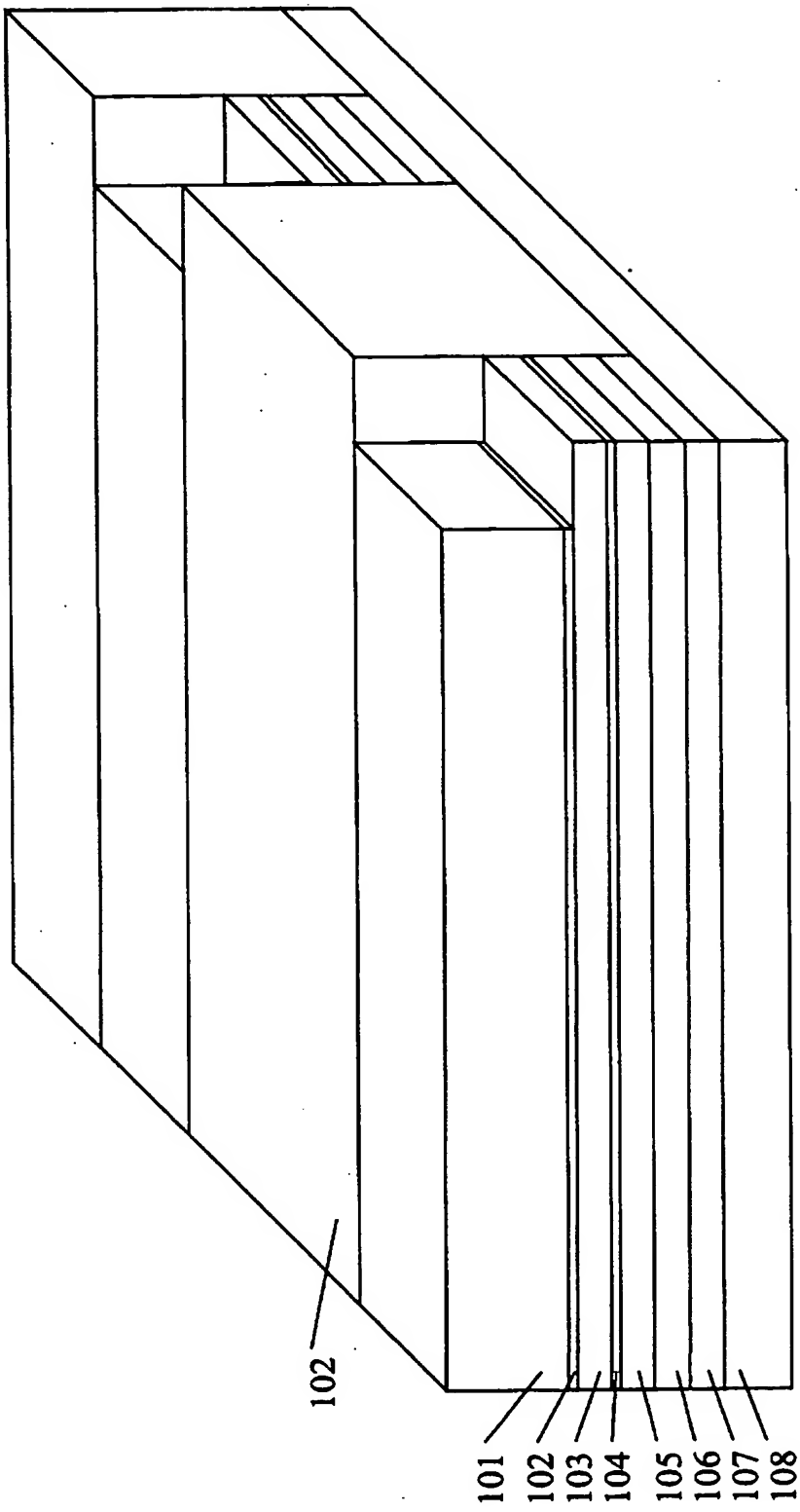


Figure 11F

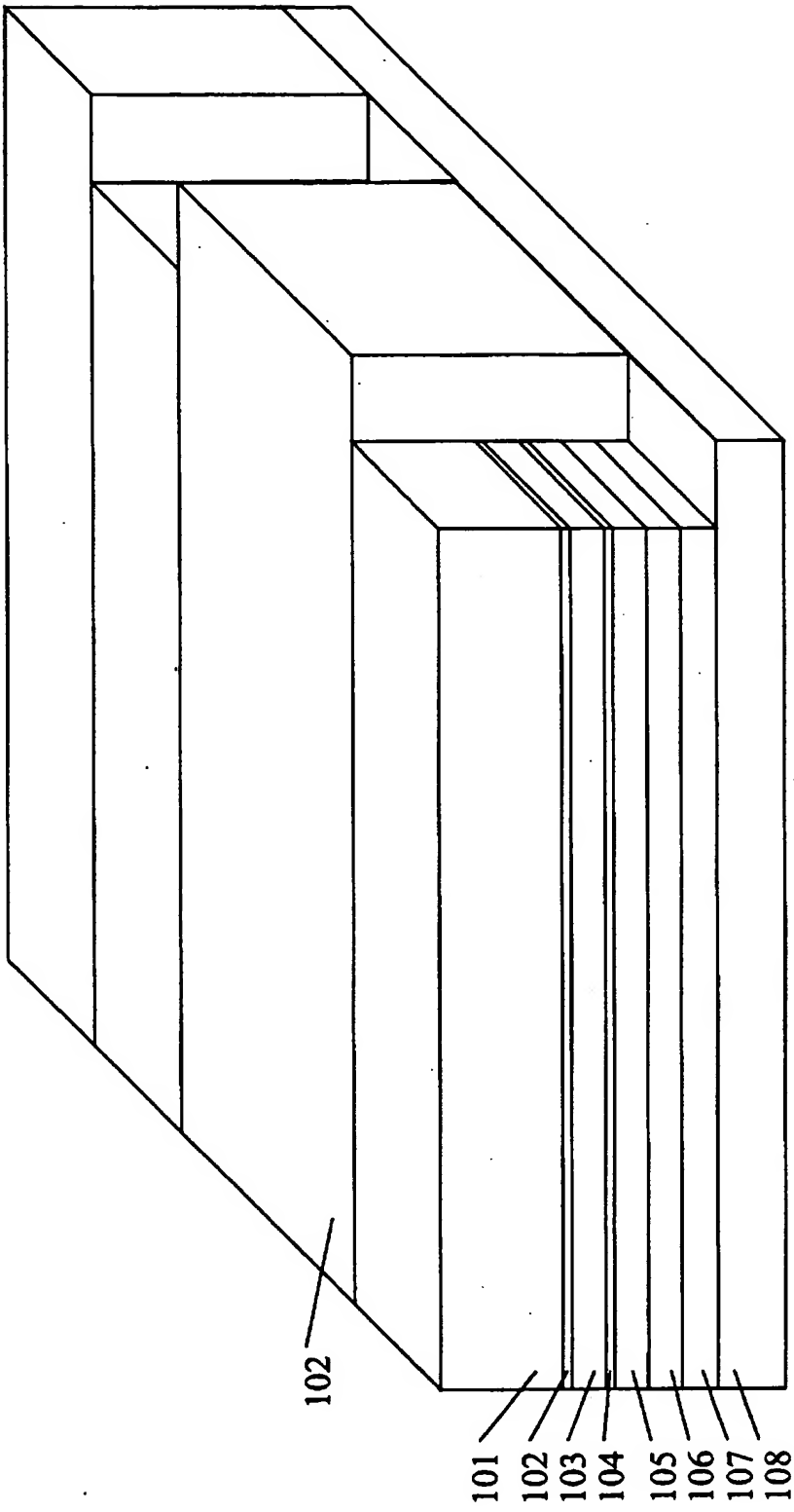


Figure 11G

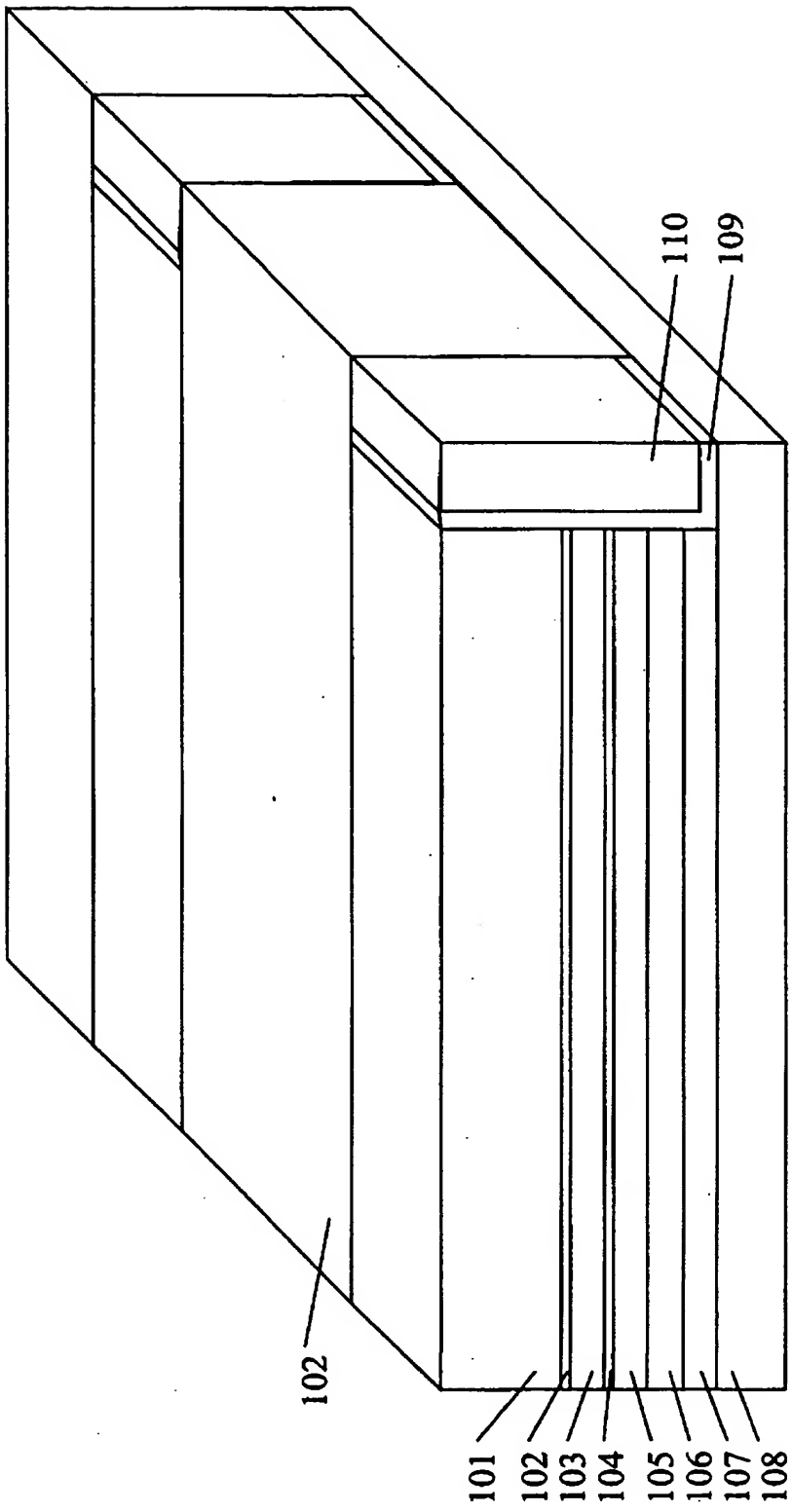


Figure 11H

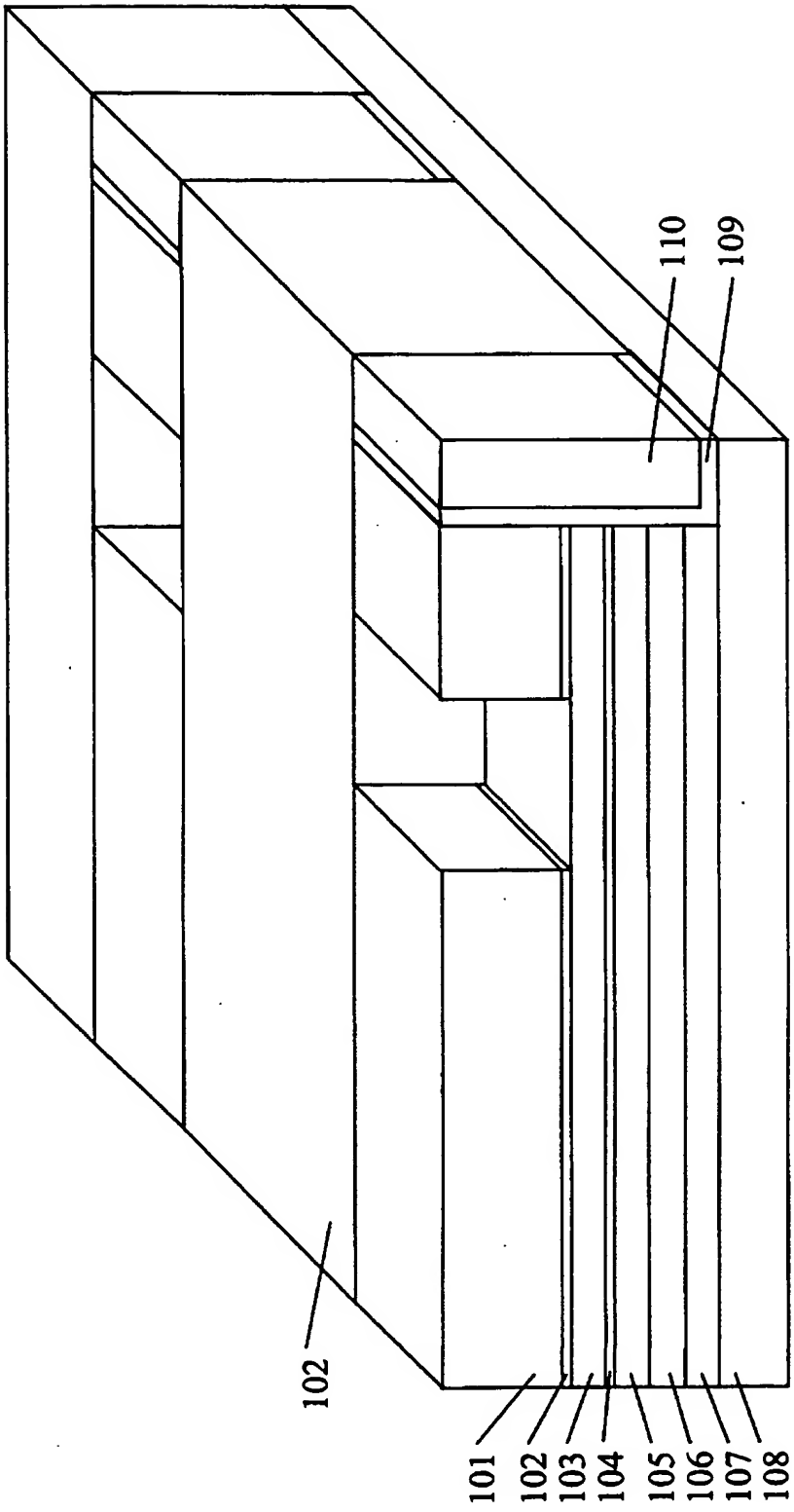


Figure 11I

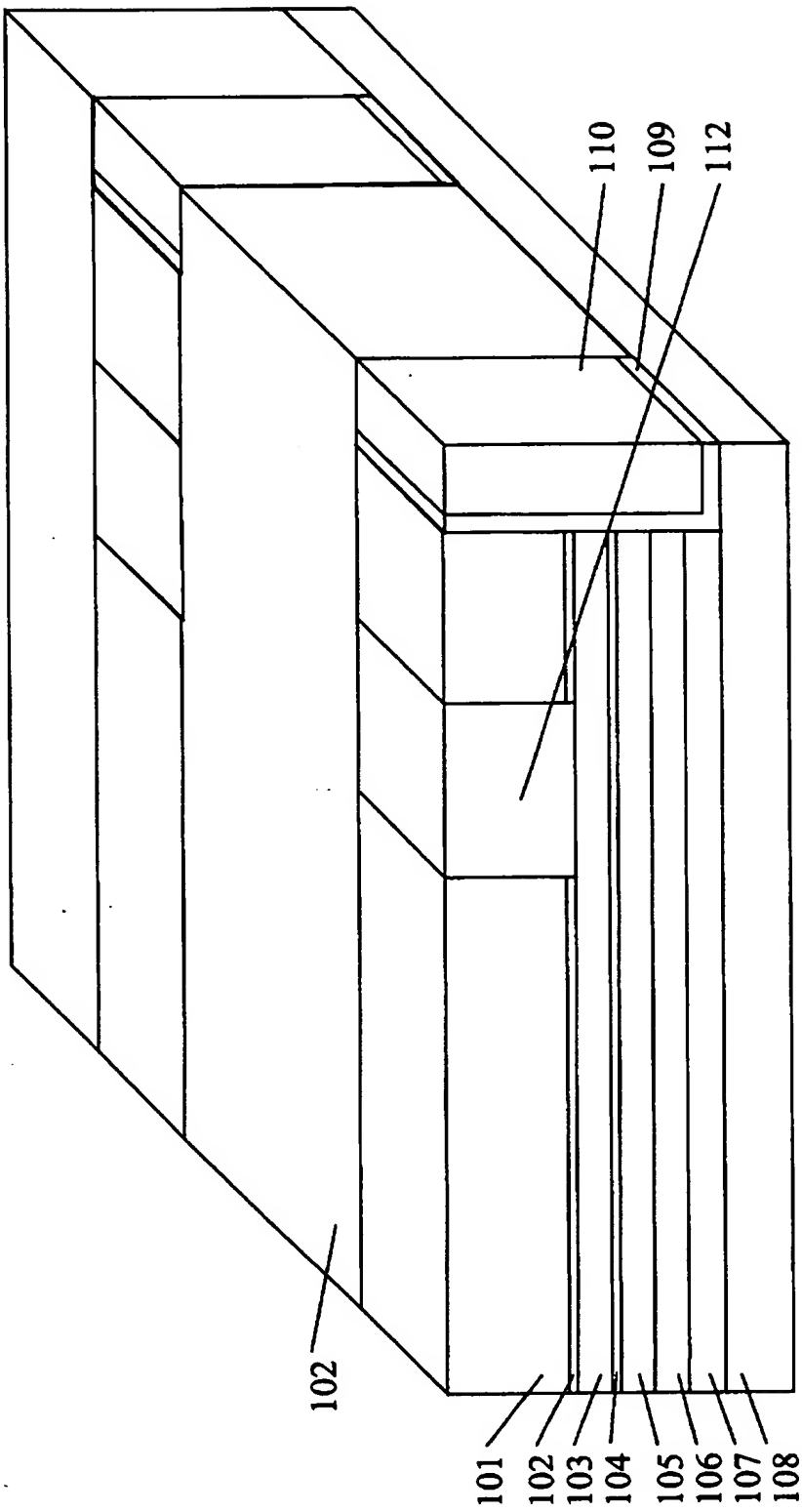


Figure 11J

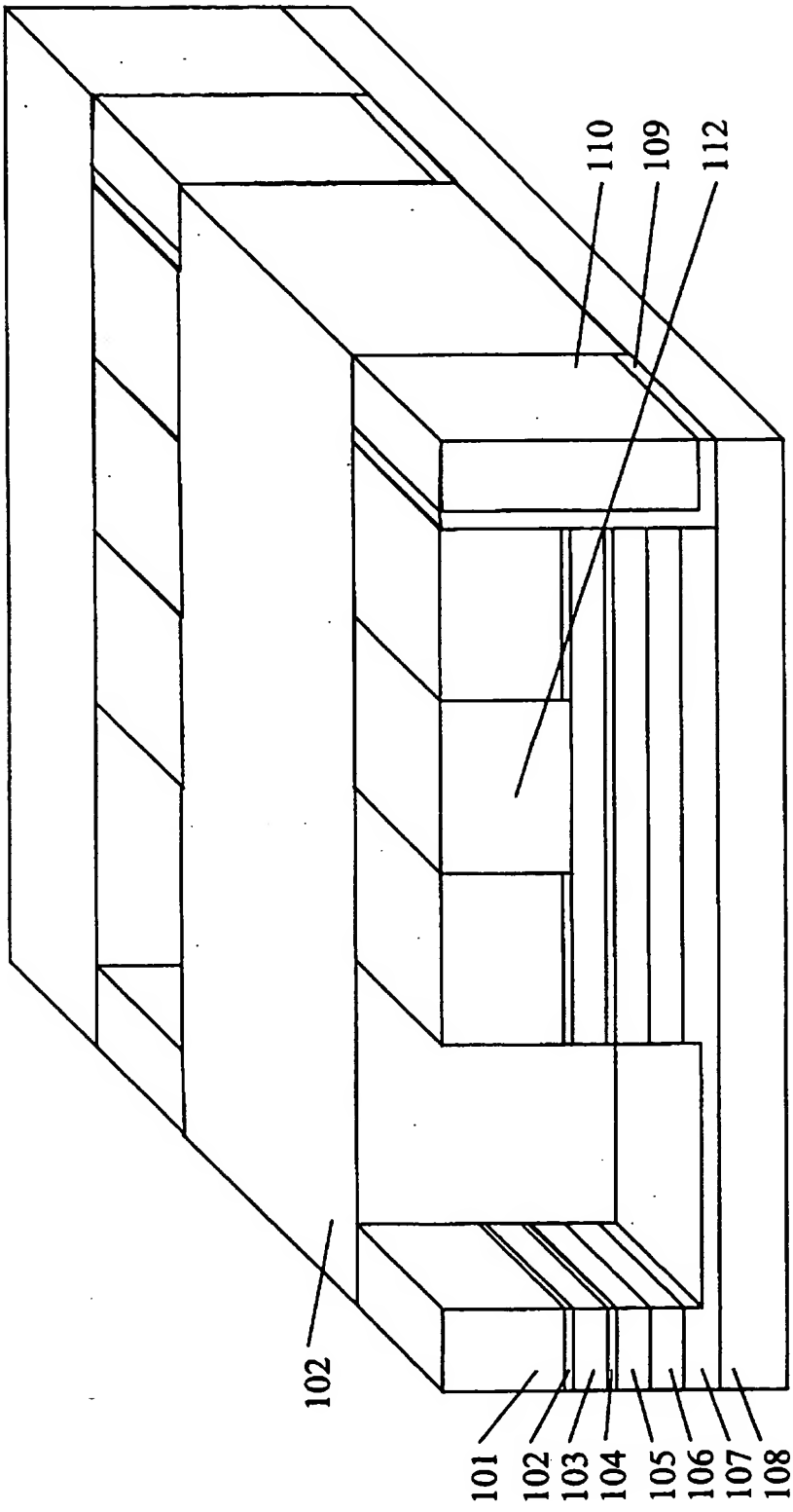


Figure 11K

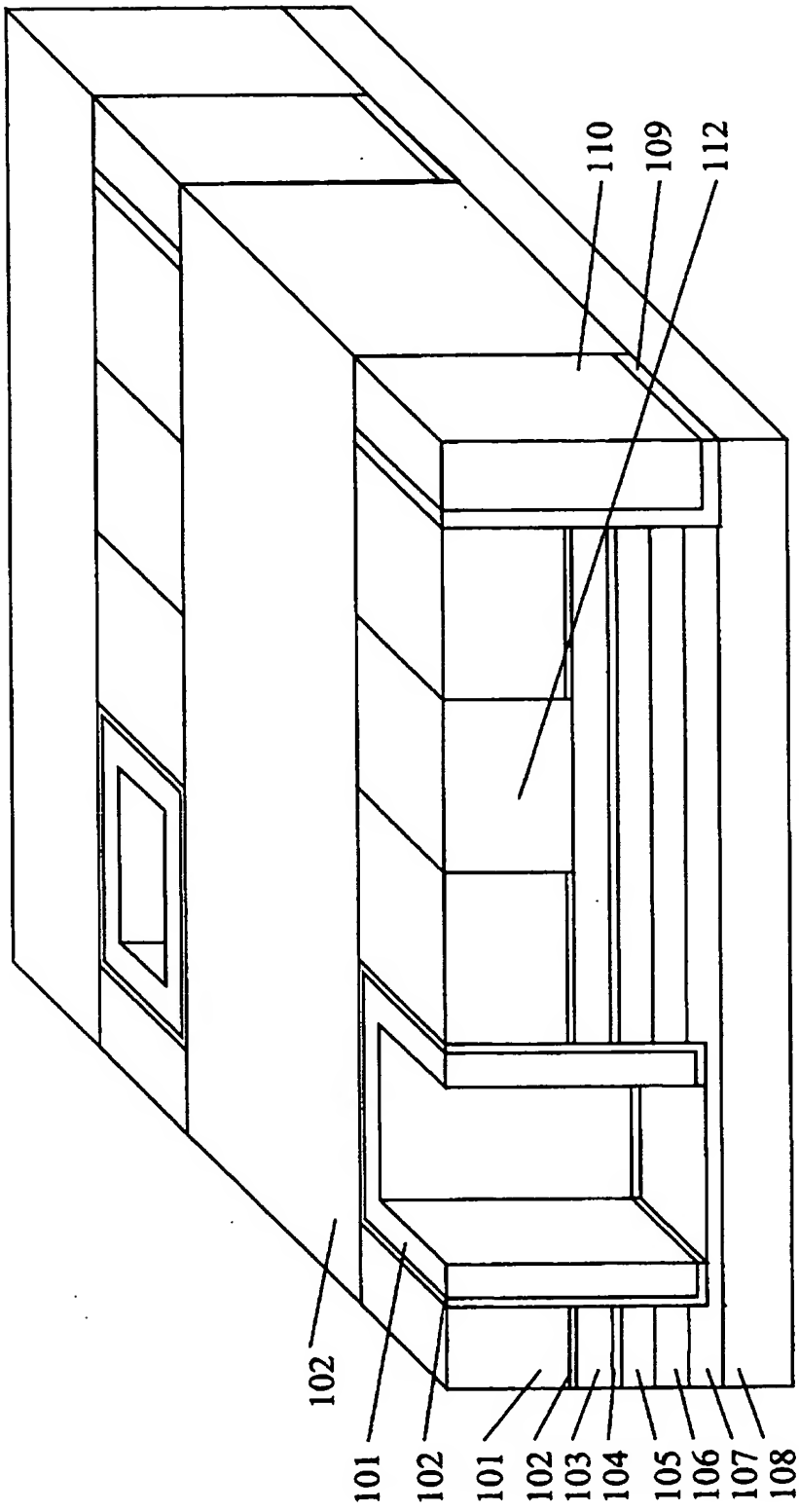


Figure 11L

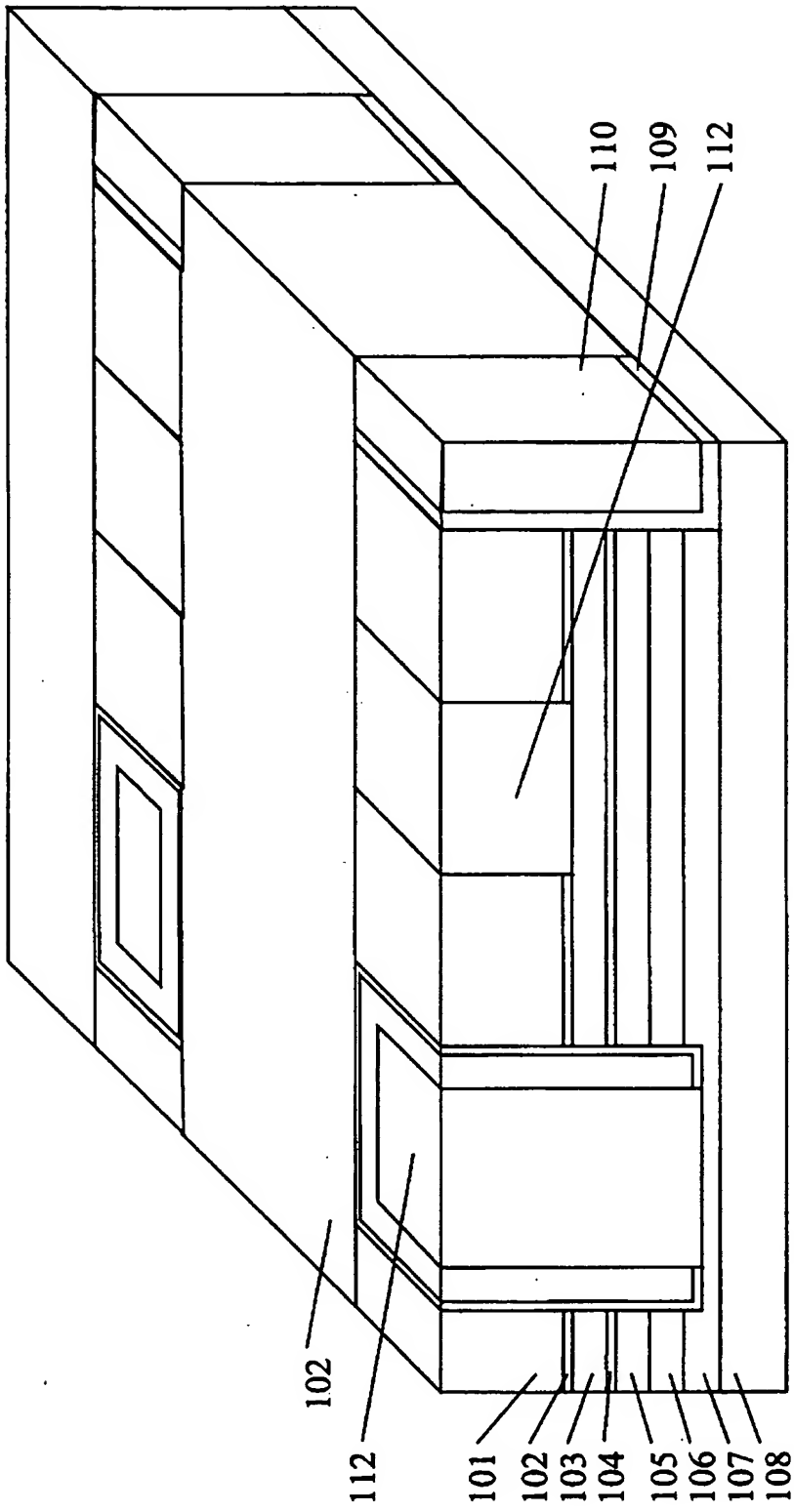


Figure 11M

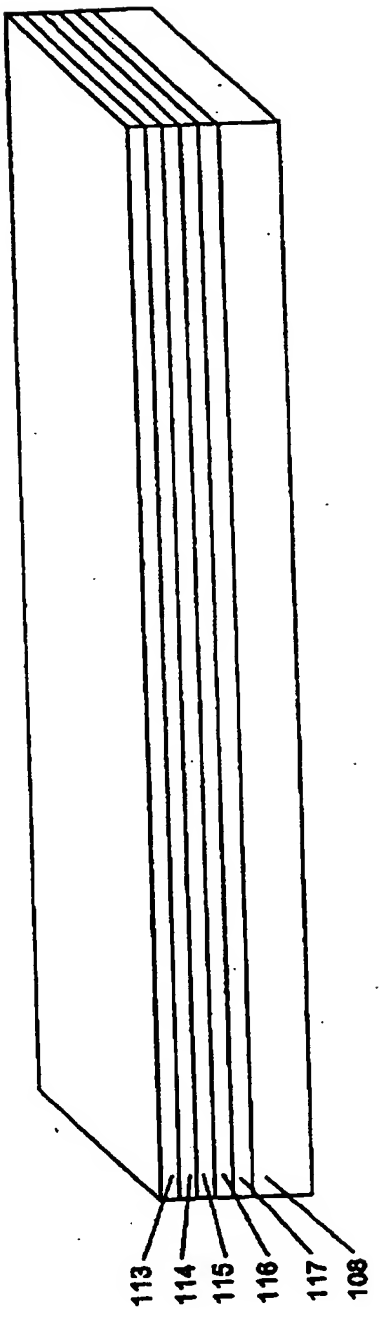


Figure 12A

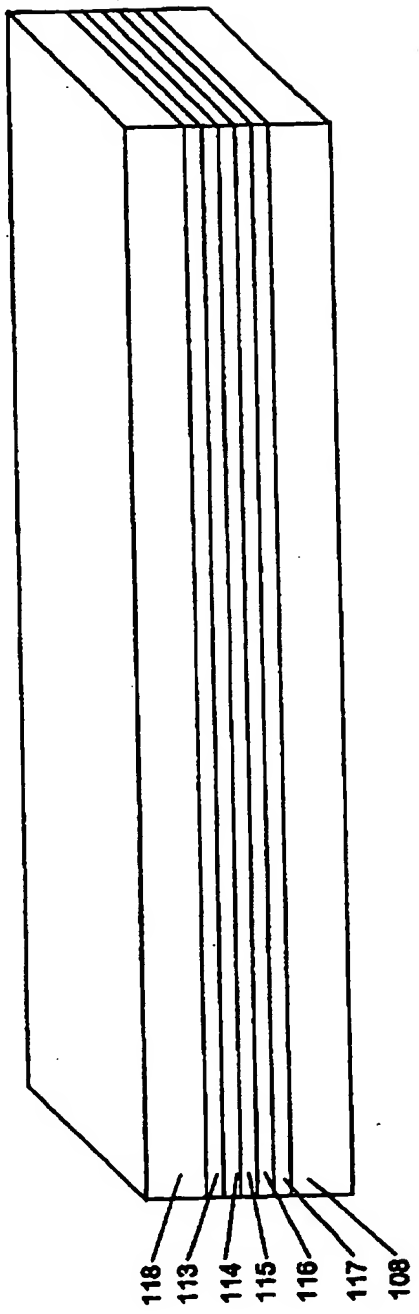


Figure 12B

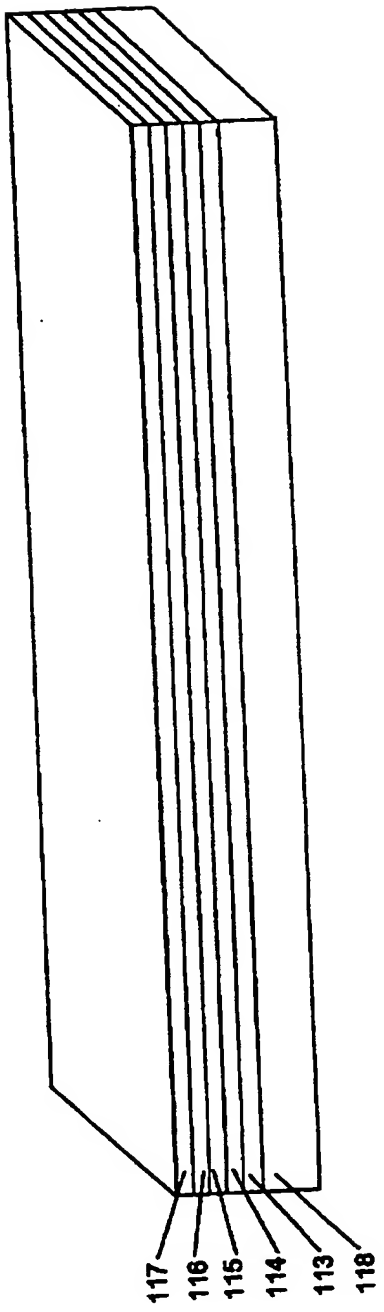


Figure 12C

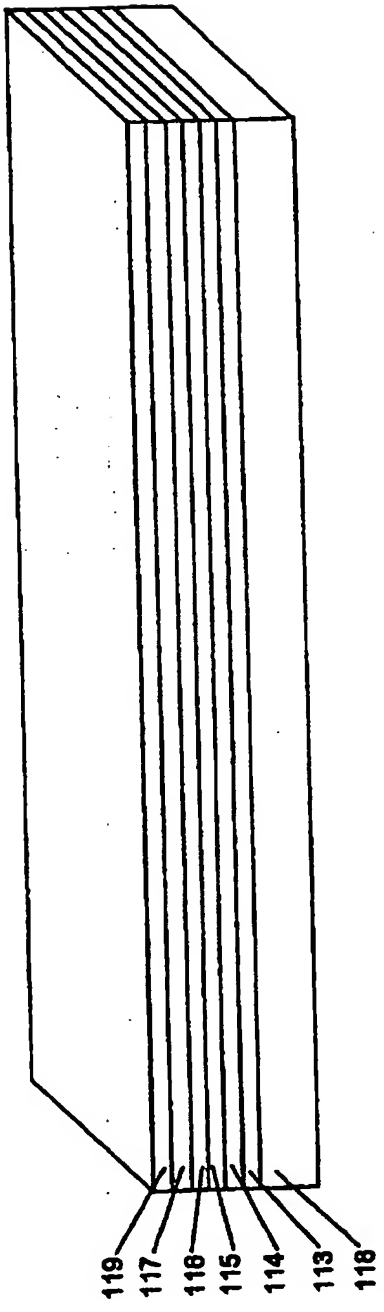


Figure 12D

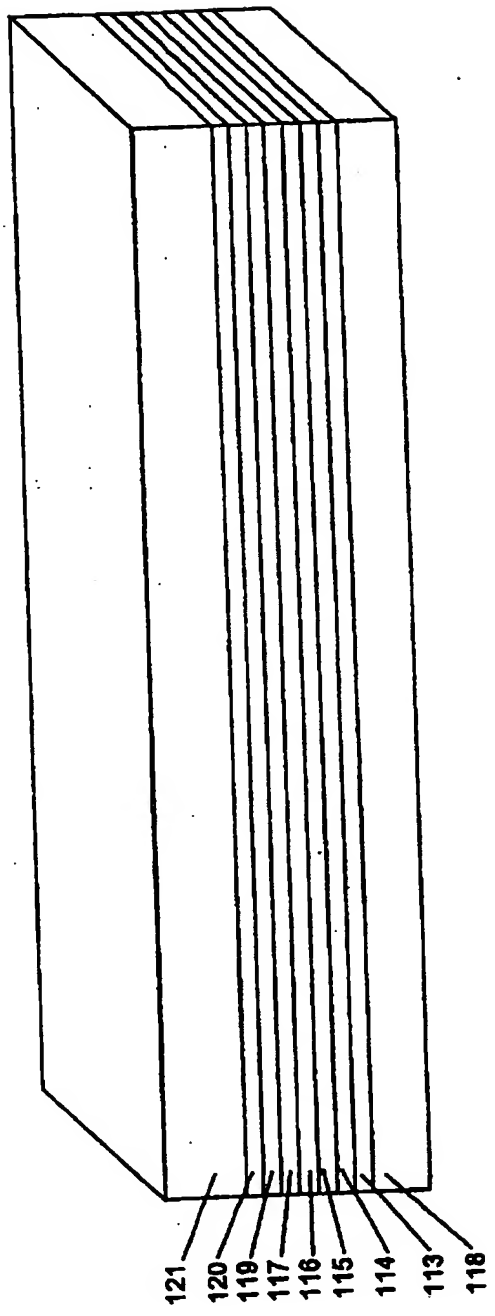


Figure 12E

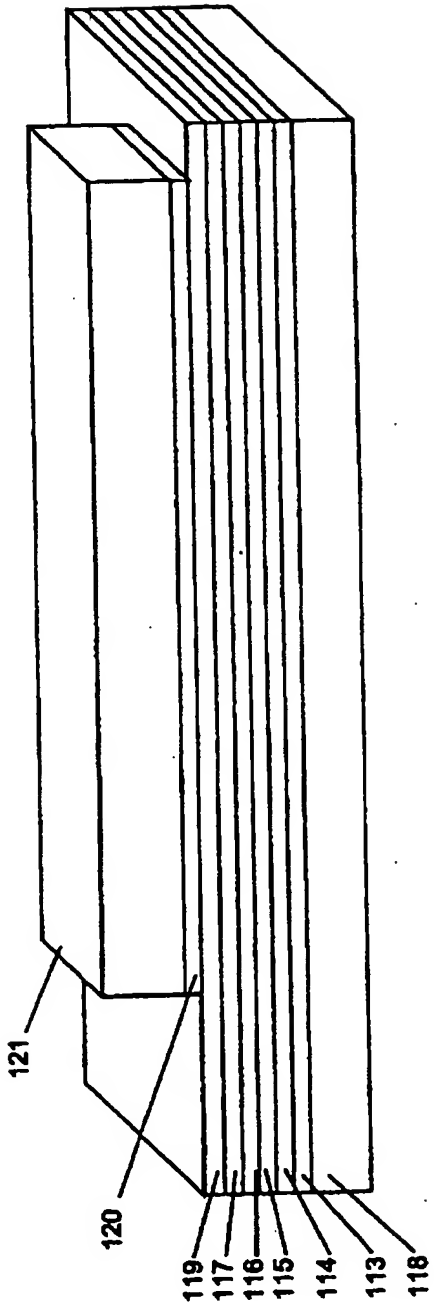


Figure 12F

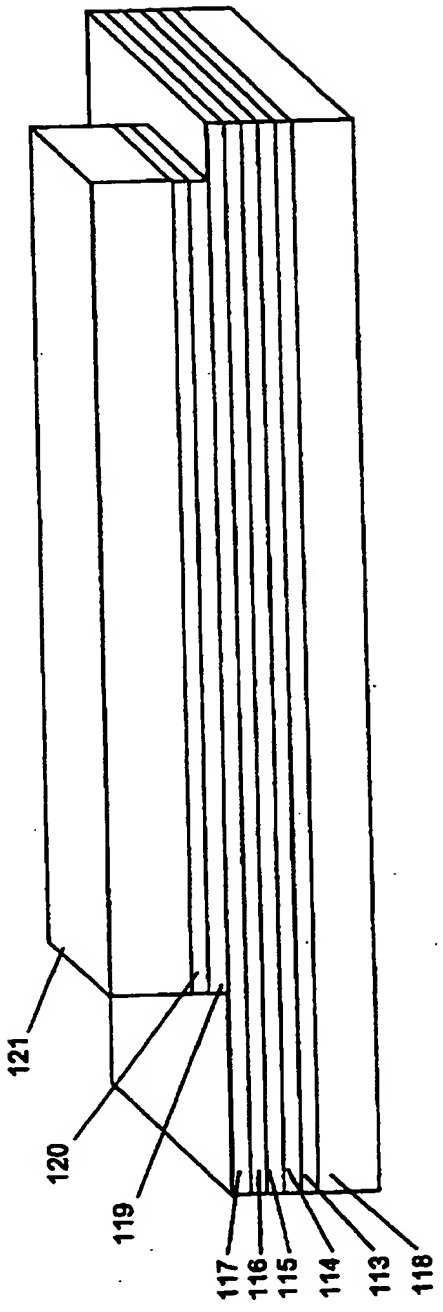


Figure 12G

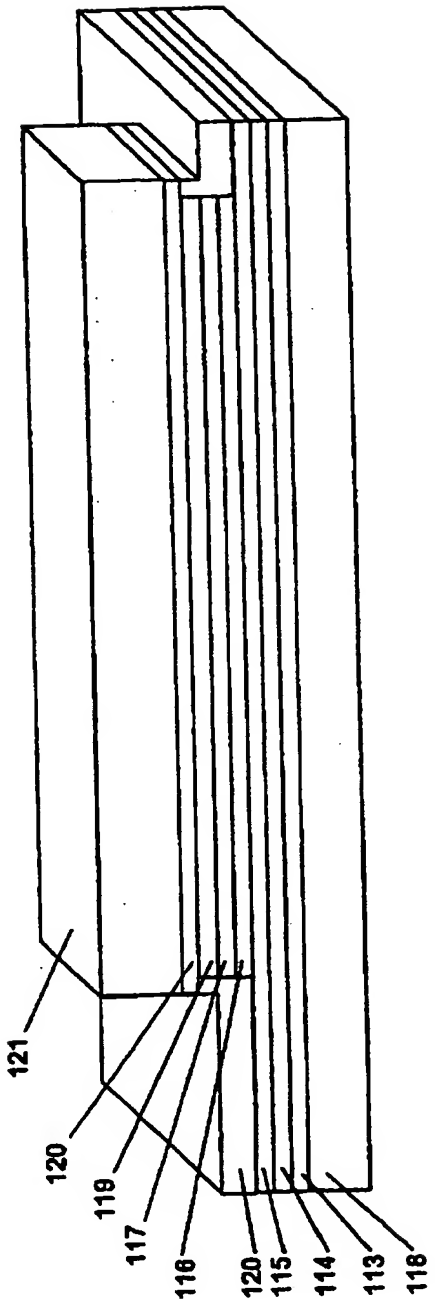


Figure 12H

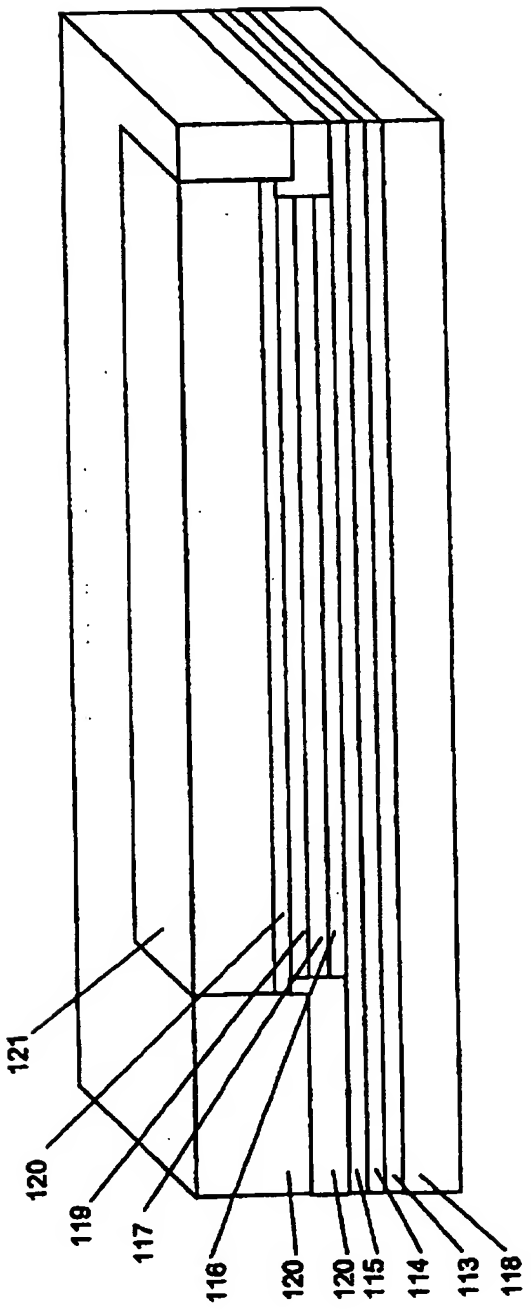


Figure 12I

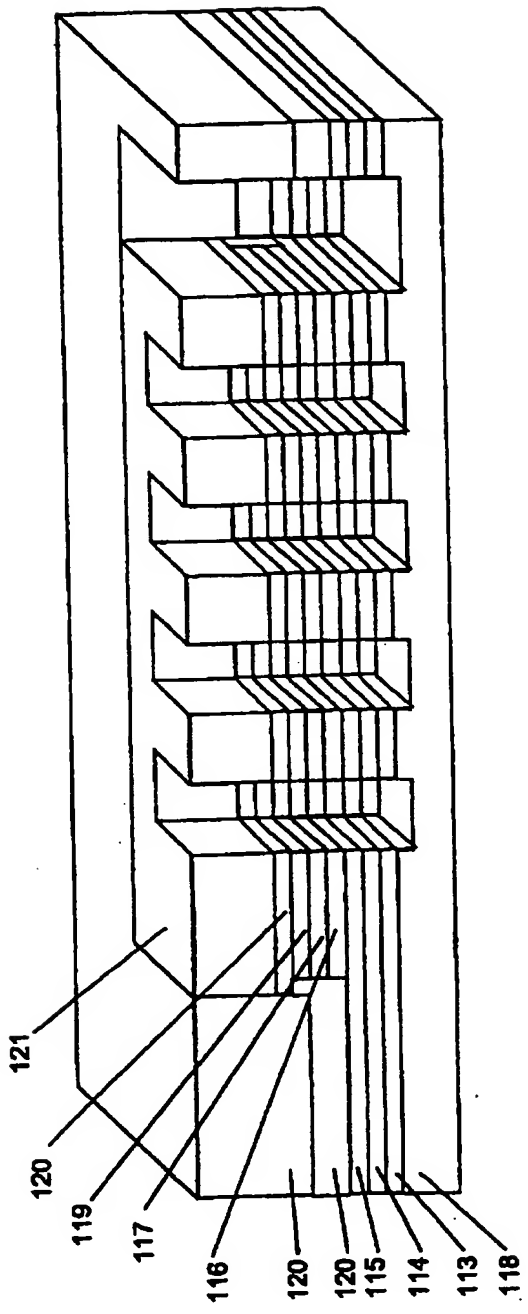


Figure 12J

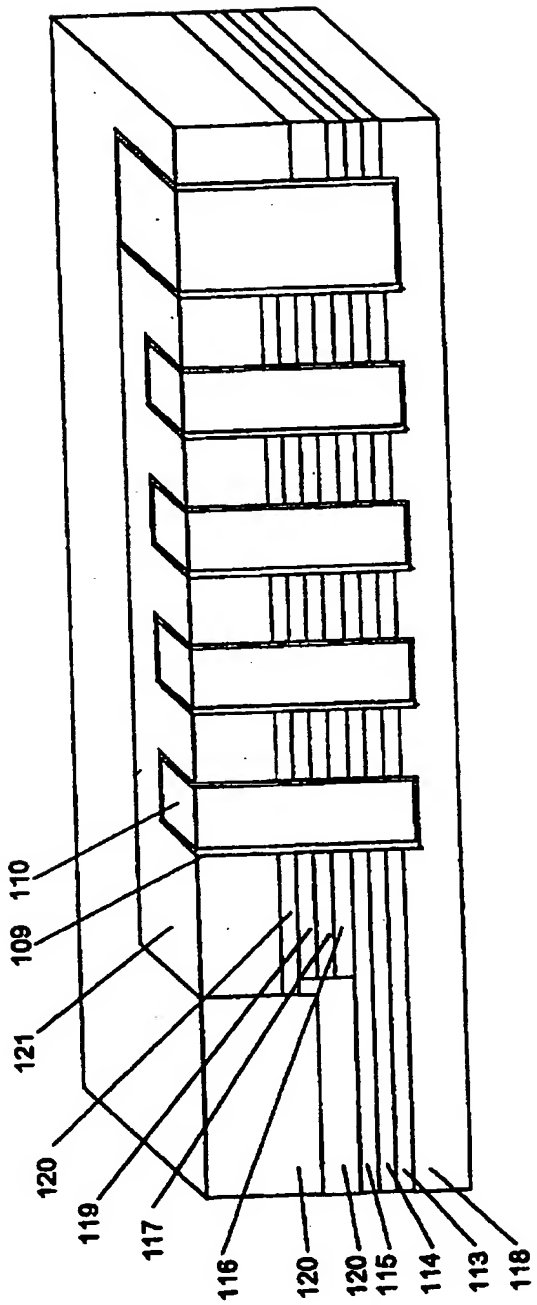


Figure 12K

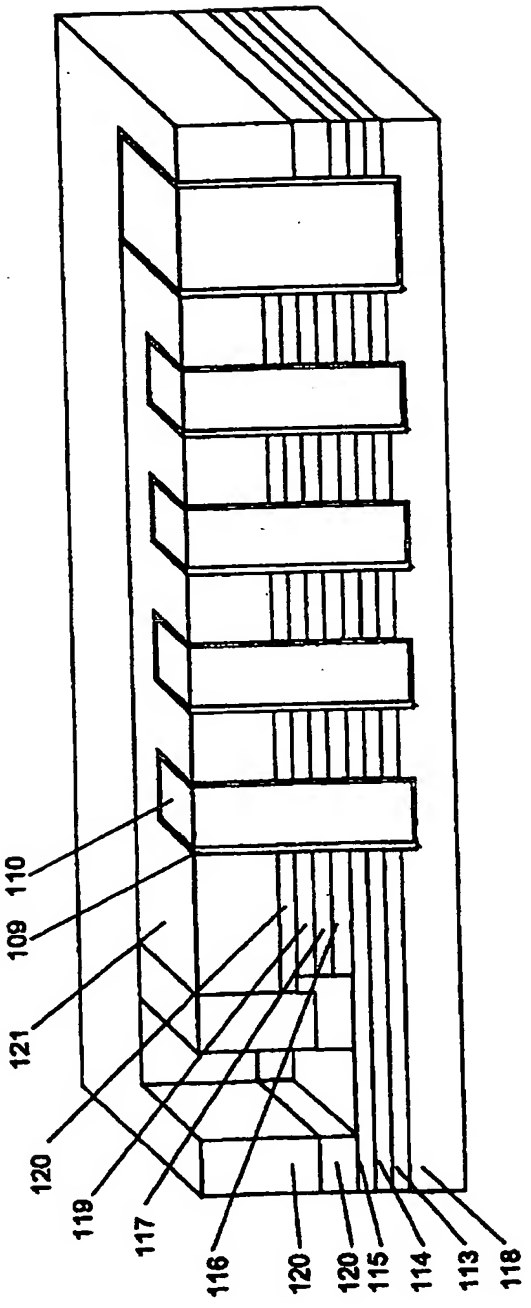


Figure 12L

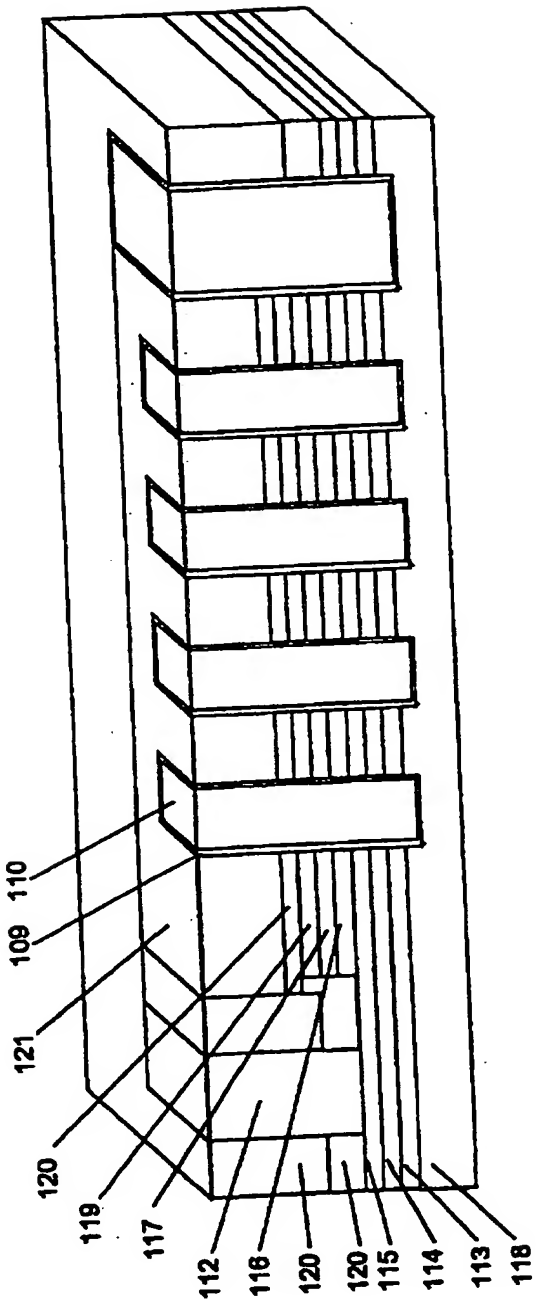


Figure 12M

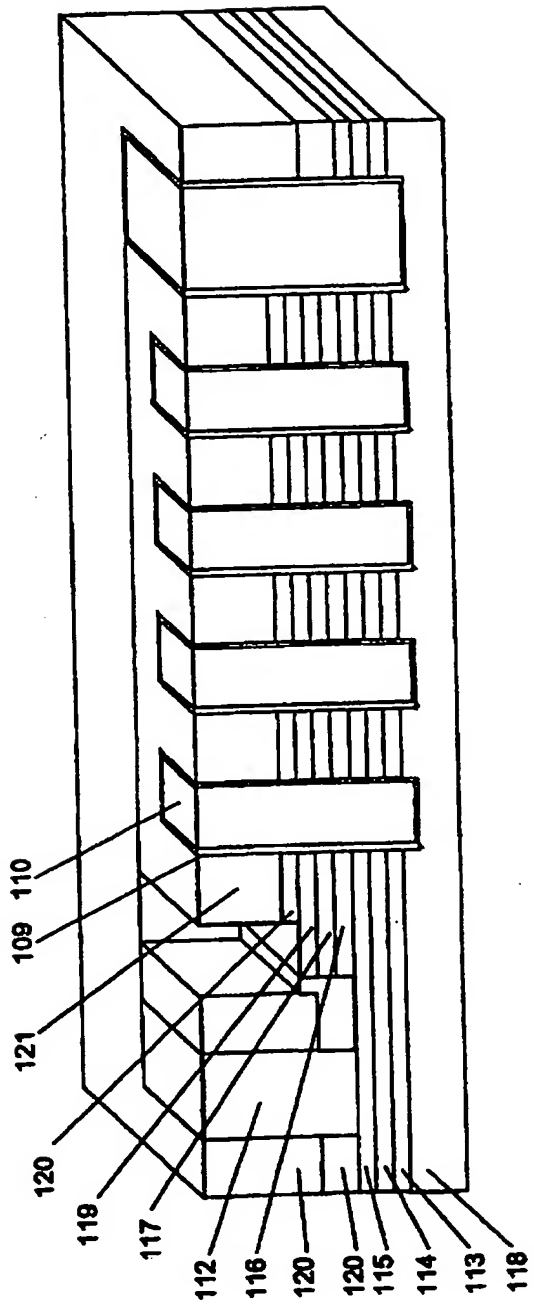


Figure 12N

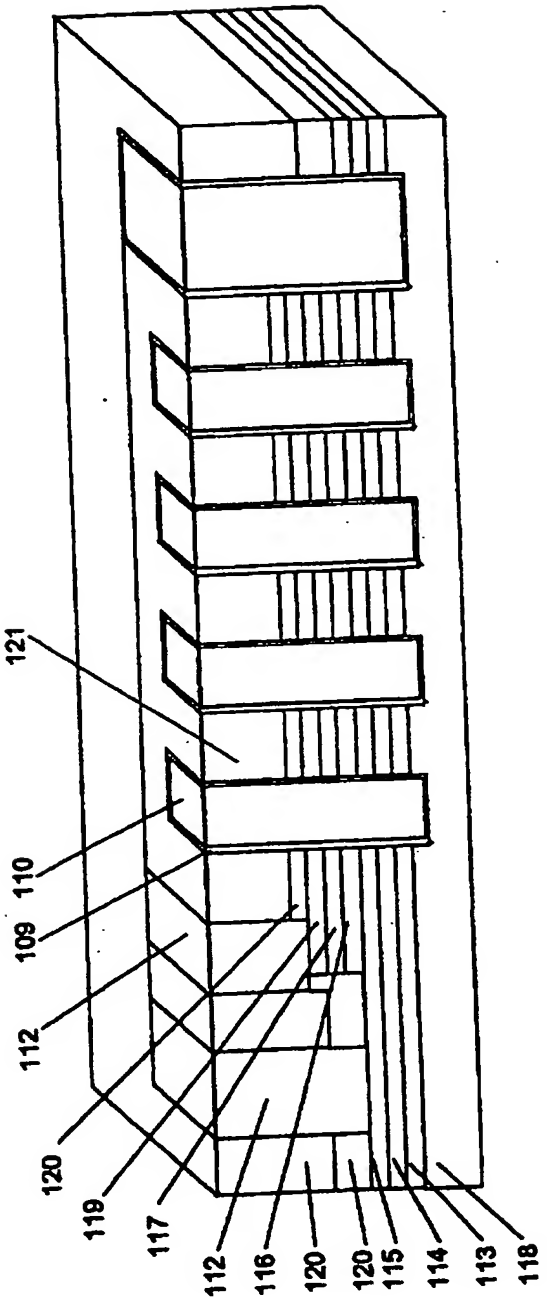


Figure 120

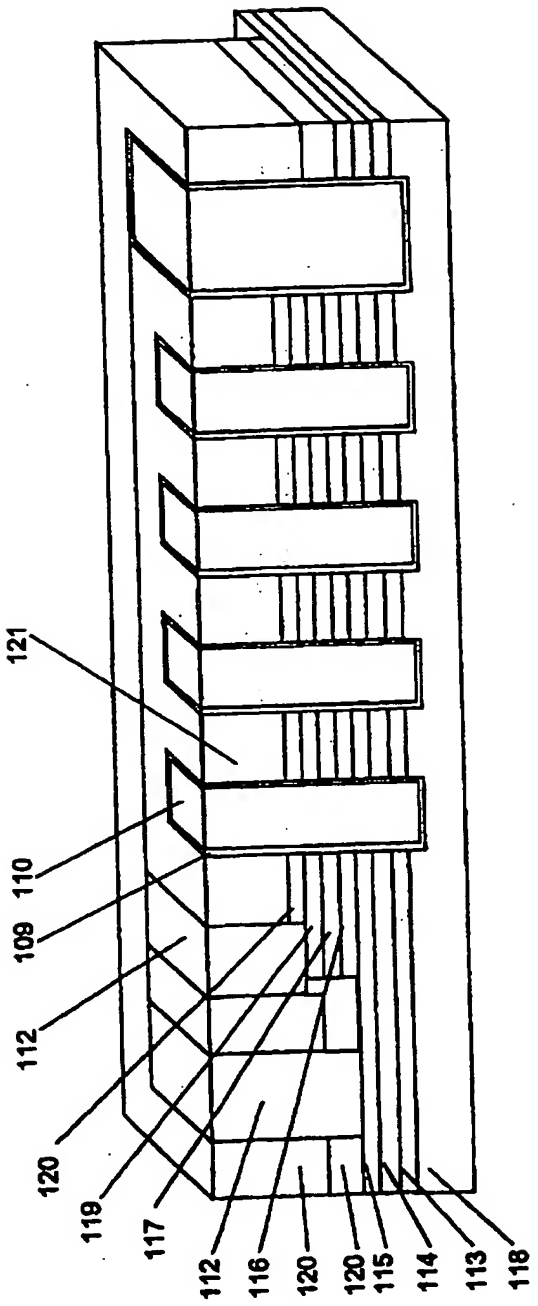


Figure 12P

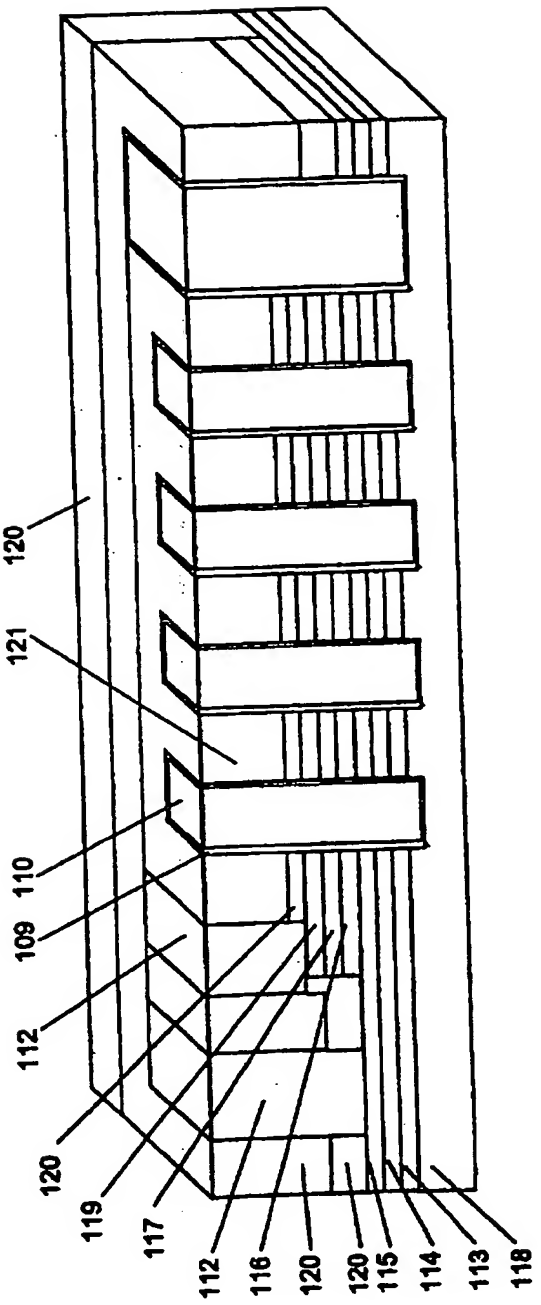


Figure 12Q

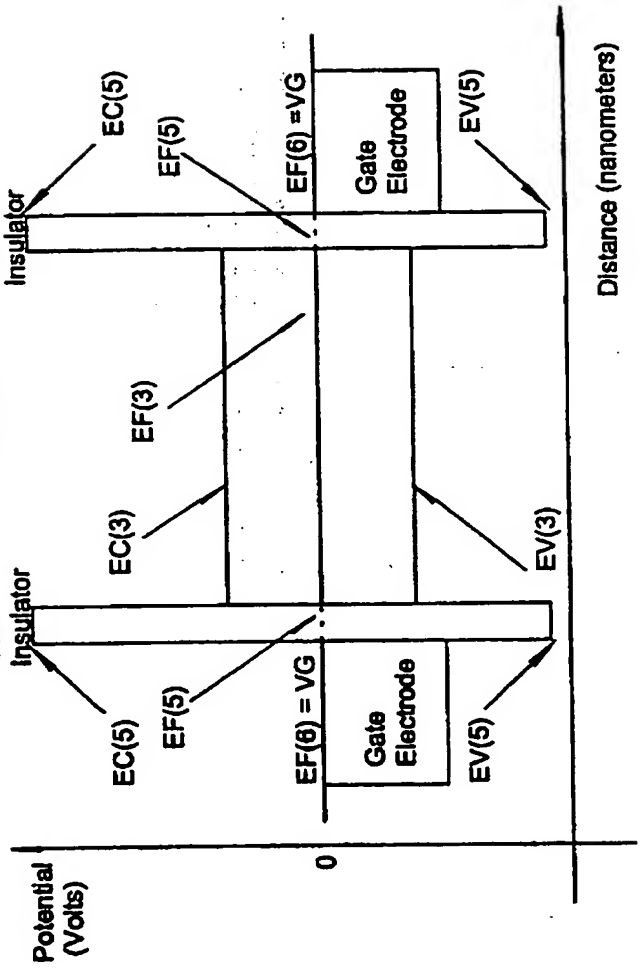

Potential (Volts)
0
Distance (nanometers)
Gate Insulator
Gate Insulator
Channel
EC(5)
EF(5)
EF(6) = VG
Gate Electrode
EV(5)
EC(3)
EF(3)
EV(3)
EC(5)
EF(5)
EF(6) = VG
Gate Electrode
EV(5)

Figure 13a

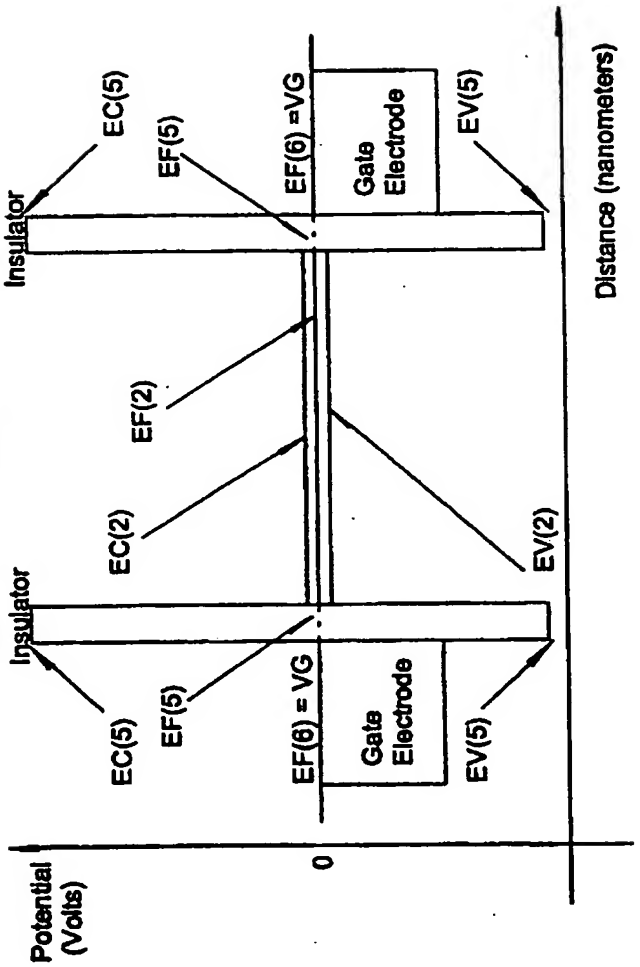

Potential (Volts)
0
Distance (nanometers)
Gate Insulator
Source
Gate Insulator
EC(5)
EF(5)
EF(6) = VG
Gate Electrode
EV(5)
EC(2)
EF(2)
EV(2)
EC(5)
EF(5)
EF(6) = VG
Gate Electrode
EV(5)

Figure 13b

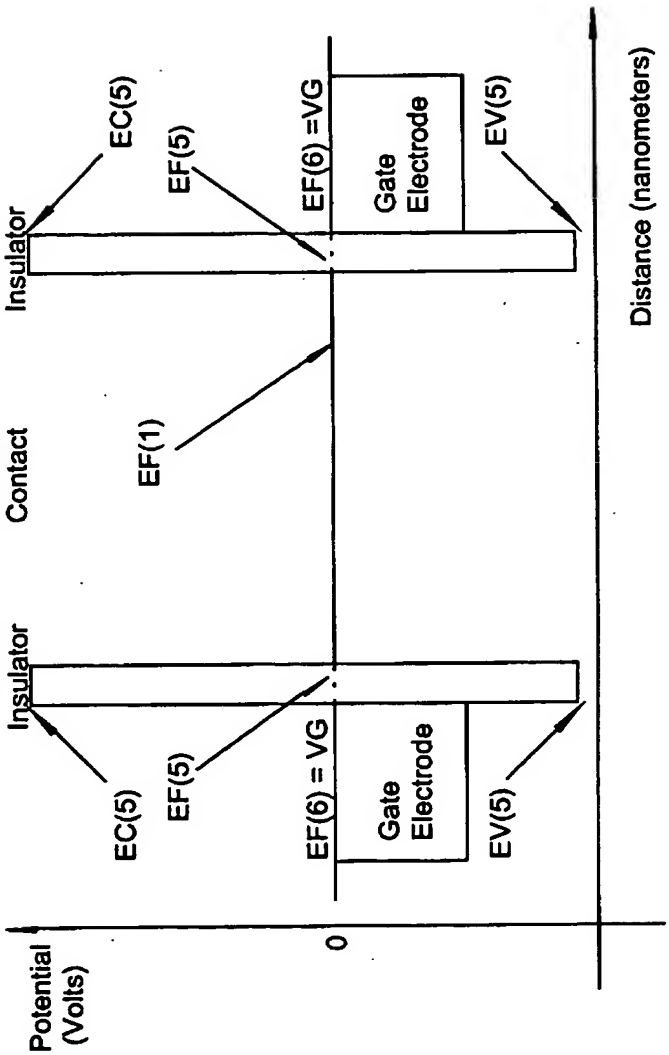

Potential (Volts)
0
Distance (nanometers)
Gate Insulator
Source Contact
Gate Insulator
EC(5)
EF(5)
EF(6) = VG
Gate Electrode
EV(5)
EF(1)
EC(5)
EF(5)
EF(6) =VG
Gate Electrode
EV(5)

Figure 13c

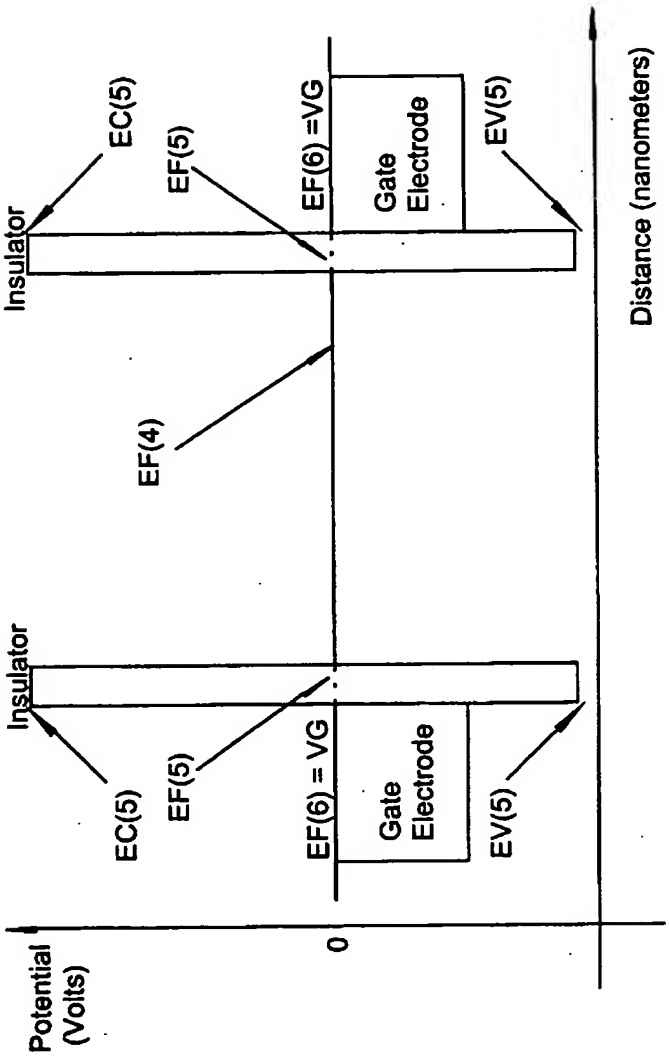

Potential (Volts)
0
Distance (nanometers)
Gate Insulator
EC(5)
EF(5)
EF(6) = VG
Gate Electrode
EV(5)
Drain
EF(4)
Gate Insulator
EC(5)
EF(5)
EF(6) =VG
Gate Electrode
EV(5)

Figure 13d

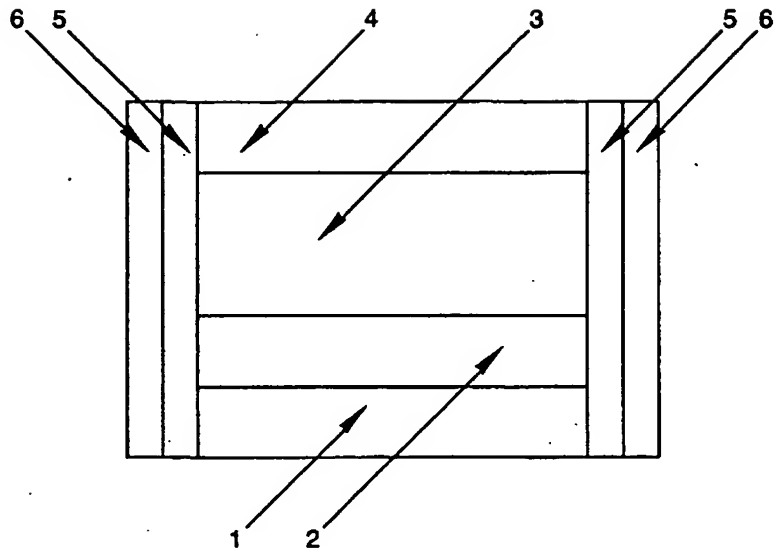


Figure 14

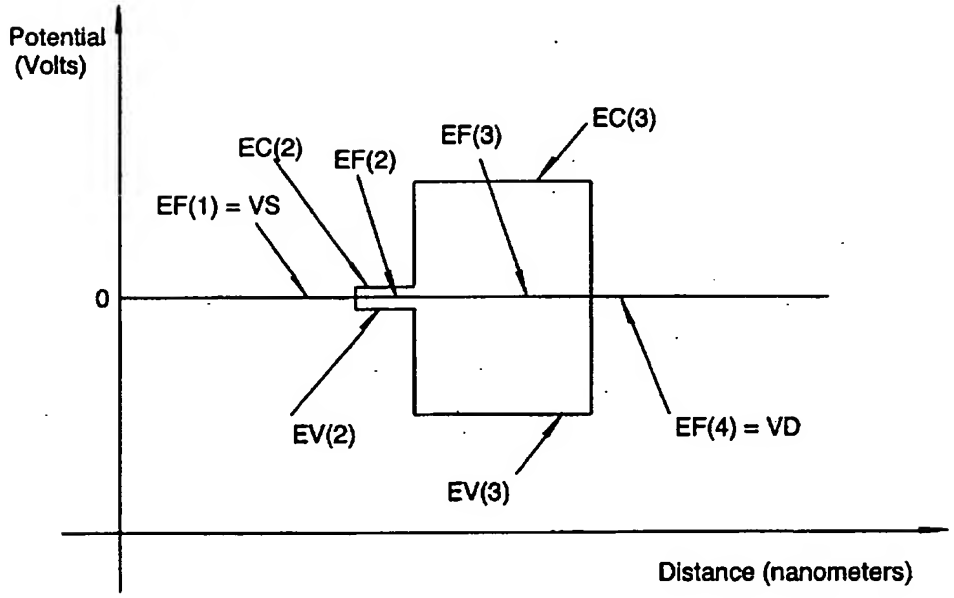


Figure 15